WAVETEK

MAINTENANCE MANUAL

# Model 90
## 20 MHz Synthesized Function Generator

For Model 90 operation information, refer to separate Operator's Manual, P/N 1006-00-0596.

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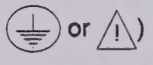
# SAFETY FIRST

**Protect yourself.** Follow these precautions:

- Don't touch the outputs of the instrument or any exposed test wire carrying the output signals. This instrument can generate hazardous voltages and currents
- Don't bypass the power cord's ground lead with two-wire extension cords or plug adapters.
- Don't disconnect the green and yellow safety-earth-ground wire that connects the ground lug of the power receptacle to the chassis ground terminal (marked with  or )
- Don't hold your eyes extremely close to an RF output for a long time. The normally nonhazardous low-power RF energy generated by the instrument could possibly cause eye injury.
- Don't plug in the power cord until directed to by the installation instructions.
- Don't repair the instrument unless you are a qualified electronics technician and know how to work with hazardous voltages.
- Pay attention to the **WARNING** statements. They point out situations that can cause injury or death.
- Pay attention to the CAUTION statements. They point out situations that can cause equipment damage.

**WARNING**

**This instrument normally contains a lithium battery. Where lithium is prohibited, such as aboard U.S. Navy ships, verify that the lithium battery has been removed.**

**Do not recharge, short circuit, disassemble, or apply heat to the lithium battery. Violating this rule could release potentially harmful lithium. Observe polarity when you replace the battery.**

## 1.1. Introduction

This manual contains information on the testing, calibration, and servicing of the Wavetek Model 90, 20 MHz Synthesized Function Generator.

## 1.2 What Is In This Manual

This manual contains the following sections:

Section 2 Routine Preventive Maintenance.
Section 3 Verification Procedure.
Section 4 Calibration Procedure.
Section 5 Circuit Description.
Section 6 Maintenance (Troubleshooting).
Section 7 The Drawing Package.
Appendix A Product Description and Specifications

## 1.3 How To Use This Manual

The purpose of the maintenance manual is to support the technician in keeping the Model 90 functioning correctly. The material in this manual is organized in such a way as to aid the service technician in identifying and isolating a problem with the unit.

Spare And Replacement Parts

Users who plan on servicing the Model 90 may choose to order spare parts from Wavetek. Each assembly contains a parts list; see the drawing package, section 7. All parts listed may be ordered directly from Wavetek. In addition, a recommended spare parts package (Wavetek part number 1200-00-3462) can be ordered from Wavetek.

### Suspected Malfunctions

If the Model 90 does not operate correctly, check the instrument setup before trying to isolate the problem; see the *Model 90 Operator's Manual.* Or, perform an Autocal on the unit to see if the instrument will correct the problem itself; see section 4 of this manual. If there is a problem, performing Autocal causes the unit to return an error message.

If the problem is known, turn to the appropriate section and correct the fault. Use the Calibration procedure, section 4, when the Model 90 appears out of calibration. Also, the Model 90 provides error messages which can guide the technician to circuit blocks within the instrument; see section 6. Use the maintenance section, section 6, to isolate failures. Section 6 does not isolate problems down to the component level, but only to the circuit block. In addition to the Maintenance section, the Circuit Description, schematics, and assembly drawings all support problem isolation.

## 1.4 The Operator's Manual

This manual does not cover the operation of the Model 90. The *Model 90 Operator's Manual* contains that information.

Product description and specifications - Section 1.
Routine Maintenance - Section 2.
Operation (both front panel and remote (GPIB)) - Section 3.

This section covers routine tasks the Service Technician may perform on the Model 90.

## 2.1 Calibration

Section 4 of this manual contains both the Autocal and Calibration Procedure instructions.

Autocal (automatic calibration) provides a quick method of calibrating the Model 90 without the use of external test equipment. Autocal automatically sets up the instrument and takes internal measurements using internal standards. The Model 90 calculates correction values and stores those values in memory. The Model 90 recalls and loads these correction values at power up. Use Autocal when Model 90 accuracy is critical, after long term instrument storage or following drastic changes in the environment. Also, perform Autocal at anytime the Service Technician believes it is necessary.

The Calibration Procedure provides a more extensive method of Model 90 calibration. The Calibration Procedure uses external test equipment and requires opening the instrument for adjustments. Use the Calibration Procedure when the Model 90 displays "CAL REQUIRED" or "FAILED AUTO CAL", after repair, Performance Verification procedure (section 3) failure, or at routine scheduled calibration.

## 2.2 Fuse Replacement

To replace the fuse (rear panel) Model 90 use the following instructions.

1. Disconnect the power cord at the instrument. Open the fuse holder cover door. Rotate the fuse-pull to the left to remove the fuse.
2. Replace the fuse with one having the same current and voltage ratings. The following table lists fuses used with different voltage ranges. Rotate the fuse pull lever back into the normal position. Insert the correct fuse in the fuse holder. Close the fuse holder cover door.

| Card | Input Vac | Fuse Position |
|---|---|---|
| 100 | 90 to 105 | 1A, 250 Vac, Slo Blo |
| 120 | 108 to 126 | 1A, 250 Vac, Slo Blo |
| 220 | 198 to 231 | 1/2A, 250 Vac, Slo Blo |
| 240 | 216 to 252 | 1/2A, 250 Vac, Slo Blo |

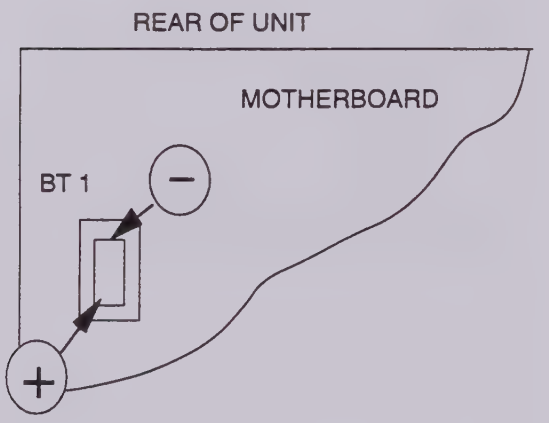
3. Connect the AC line cord to the mating connector at the rear of the unit and power source.

## 2.3 Battery Replacement

The Model 90 contains a Lithium battery (Panasonic BR-2/3A or equivalent) to power the unit's memory when power is off. This battery life is typically greater than three years. At power on, the Model 90 checks the battery's condition as part of the power-on Self-test. If Self-test detects a low battery, the display shows "LOW BAT X.XXXV". Replace the battery otherwise the contents of the memory could be lost when power is turned off.

To replace the battery,

1. Remove the top cover and shield. Remove the four screws in the top and the one screw at the rear of the cover. Slide the cover back.
2. With the power ON, replace the old battery, as shown in the following illustration, with a new battery. Observe the polarity of the battery when installing it. If the power is turned off while replacing the battery, all contents of the RAM will be lost.




3. Replace the top cover and shield. Secure them using the four screws in the top and the one screw in the rear of the cover.

## 2.4 Fan Maintenance

The Model 90 fan contains a filter which should be cleaned about every month. Clean the filter more often if the unit is used in a dusty environment.

To clean the Filter,

1. Disconnect the Model 90 from the primary power source.
2. Using a screwdriver, gently pry off the Filter's grill.
3. Remove the foam filter.
4. Clean the foam filter using a mild soapy solution. Thoroughly rinse the filter, and allow it to dry.
5. Place the filter back in the unit, and snap in the Filter's grill.
6. Connect the Model 90 to the primary power source.

## 3.1 Performance Verification

Performance verification tests the operation of every selectable parameter and input/output connector. Furthermore, it verifies the correct operation within each major specification. Use this procedure after a manual calibration (section 4) to confirm the units accuracy. All data obtained during the performance verification should be permanently recorded for future reference. The Verification Form, located at the end of this appendix, can be used as a master to generate copies. This procedure assumes the person making the tests has a good working knowledge of the Model 90 operation. For information on Model 90 operation, refer to Section 3, Operation of the Model 90 Operator's Manual.

Required Test Equipment - Table 3-1 lists the test equipment required to perform the performance verification procedure. Always keep test equipment interconnecting cables as short as possible.

**Table 3-1. Required Test Equipment**

| Test Equipment | Recommended Model |
|---|---|
| Scope | Tektronix 2465 or equivalent. |
| THD Analyzer | Hewlett Packard 8903B or equivalent. |
| DMM | Wavetek Model 1062 or equivalent. |
| Signal Source | Wavetek Model 23 or equivalent. |
| Counter/Timer | Hewlett Packard 5335A or equivalent. |
| Phase Meter | Hewlett Packard 3575A or equivalent. |
| Signal Source | Wavetek Model 178 or equivalent (Option 001) |

### Frequency Range

1. Initialize the Model 90 by pressing the SHIFT and RESET ALL key; see table 3-2 for a list of default parameters.

**Table 3-2. Model 90 Default Conditions**

| Key | Condition |
|---|---|
| Frequency | 1kHz (1ms) |
| Amplitude | 5Vpp (2.5 Vp, 1.768 Vrms, 18 dBm) |
| Display | 16 |
| Mode | Continuous |
| Offset | 0V |
| Symmetry | 50% |
| Store | Last location stored |
| Recall | Last location stored |
| Phase | 0° (0 radians) |
| Trigger/Lock Source | Internal |
| Burst Counter | 5 |
| Function | Sine |
| Sweep Mode | Continuous Sweep |
| Sweep Start | 1kHz |
| Sweep Stop | 10 kHz |
| Time | 1s Sweep |
| Linear/Logarithmic | Linear Sweep |
| Trigger Frequency | 100 Hz |
| On/Off (Function Outputs) | Output Off (50Ω indicator flashes) |
| Select output | 50Ω, Unbalanced |
| Knob | Disabled (ENABLED Indicator off) |

Note: The following keys are not affected by the RESET ALL key:

Calibrate
Man trigger
Local
*GPIB Address*

2. Connect the Model 90 and test equipment as shown in figure 3-1.

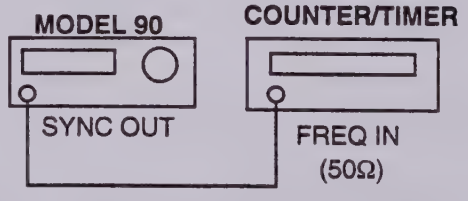



**Figure 3-1. Frequency/Symmetry Measurement Setup**

3. Program the frequency to the top frequency of each of the top seven decade frequency ranges (Verification Form - Frequency Ranges Synthesized Settings) using the FREQUENCY key and knob/key-

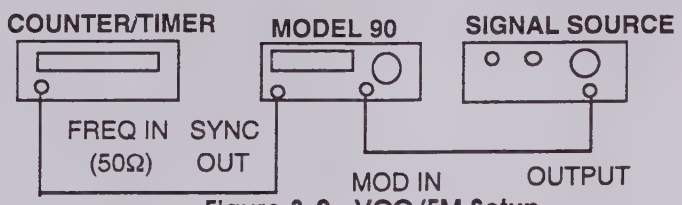


Figure 3-2. VCG/FM Setup

pad. Check the synthesized frequency accuracy per the Specified Value , and record the data on the form.

4. Select Continuous mode (MODE key), and set the frequency using the FREQUENCY key and knob/keypad (Verification Form - Unlocked FM: Settings). Next, change to the FM mode (MODE key) and measure the frequency. Record the results on the form. Repeat the range measurements for all seven upper frequency ranges.

5. Select Continuous mode (MODE key), and set the frequency using the FREQUENCY key and knob/keypad (Verification Form - Unlocked Continuous Settings). Measure the frequency, and record the results on the form. Repeat the range measurements for the three lower frequency ranges.

### Frequency Resolution

1. Initialize the Model 90 by pressing the SHIFT and RESET ALL key; see table 3-2 for a list of default parameters.

2. Connect the Model 90 and test equipment as shown in figure 3-1.

3. Set the Model 90 frequency as listed in the Verification Form - Frequency Resolution Settings using the FREQUENCY key and knob/keypad. Check the synthesized frequency accuracy per the Specified Value, and record the data on the form.

### Symmetry

1. Initialize the Model 90 by pressing the SHIFT and RESET ALL key; see table 3-2 for a list of default parameters.

2. Connect the Model 90 and test equipment as shown in figure 3-1.

3. Program the symmetry as listed in the Verification Form - Symmetry Settings using the SHIFT and SYMMETRY keys and knob/keypad. Check the symmetry accuracy per the Specified Value. The specified value represents the time in µs for the negative half of the cycle. Record the data on the form.

### VCG/FM

1. Initialize the Model 90 by pressing the SHIFT and RESET ALL key; see table 3-2 for a list of default parameters.

2. Connect the Model 90 and test equipment as shown in figure 3-2.

3. Set the signal source for 0 Volts dc output. Set the Model 90 for FM mode (MODE key). Measure the Center Frequency as per the Specified Value (1kHz ± 3% frequency), and record the data on the form.

4. Set the signal source for +5 Volts dc output. Measure the Deviation Frequency as per the Specified Value (2kHz ±3%), and record the data on the form.

### Waveforms

1. Initialize the Model 90 by pressing the SHIFT and RESET ALL key; see table 3-2 for a list of default parameters. Press the ON/OFF key to turn on the output.

2. Connect the Model 90 and test equipment as shown in figure 3-3. Connect the Model 90 SYNC OUT to the scope's trigger input.

3. Set the Model 90 to the sine function (FUNCTION key). Verify the scope displays the sine wave (Verification Form - Waveform Setting Sine Wave), and record the results as per the Specified Value (Yes or No) on the form. Repeat this step for the triangle and square waves, as well as dc (Verification Form - Waveform Setting Triangle Wave, Square Wave, and DC).

### Sweep

1. Initialize the Model 90 by pressing the SHIFT and RESET ALL key; see table 3-2 for a list of default

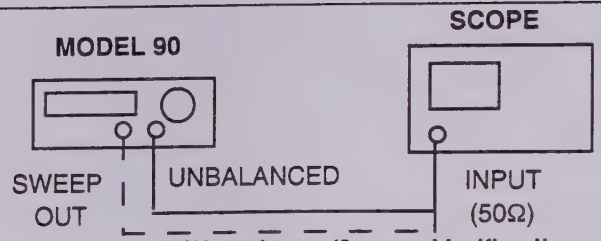


Figure 3-3. Waveforms/Sweep Verification

parameters. Press the ON/OFF key to turn on the output.

2. Connect the Model 90 and test equipment as shown in figure 3-3. Connect the Model 90 SYNC OUT to the scope's trigger input.
3. Set the Model 90 to the Sweep Mode (MODE key). Set the Sweep Mode to Continuous Sweep (SWEEP MODE key). Verify the scope displays a sweep output (1kHz to 10 kHz, 1 second sweep), and record the results on the form (Verification Form - Sweep Setting Sweep Output).
4. Connect the Sweep Out to the scope input. Verify the scope displays a 1 second sweep ramp (600Ω impedance), and record the results on the form (Verification Form - Sweep Setting Sweep Output).

### Continuous Mode

1. Initialize the Model 90 by pressing the SHIFT and RESET ALL key; see table 3-2 for a list of default parameters. Press the ON/OFF key to turn on the output.
2. Connect the Model 90 and test equipment as shown in figure 3-3. Connect the Model 90 SYNC OUT to the scope's trigger input.
3. Verify the scope displays a continuous 5Vpp sine wave. Record the results (Record Yes of No) on the form (Verification Form - Continuous Mode Setting Continuous 5Vpp Sine).

### Triggered Mode

1. Initialize the Model 90 by pressing the SHIFT and RESET ALL key; see table 3-2 for a list of default parameters. Press the ON/OFF key to turn on the output.
2. Connect the Model 90 and test equipment as shown in figure 3-4. Connect the Model 90 SYNC OUT to the scope's trigger input.
3. Set the Model 90 to the (Internal) Triggered mode (MODE key). Internal trigger is the default. Verify the scope displays an internally triggered 5Vpp sine wave. Record (Record Yes or No) the results on the form (Verification Form - Triggered Mode Setting Internal Triggered Sine Wave).
4. Set the Model 90 to the External Triggered mode (TRIG/LOCK key). Set the signal source for a 100 Hz TTL square wave. Connect the signal source output to the TRIG/LOCK IN connector. Externally trigger the scope with the signal source output.
5. Verify the scope displays an externally triggered 5Vpp sine wave. Record the results on the form (Verification Form - Triggered Mode Setting External Triggered Sine Wave).

### Gated Mode

1. Initialize the Model 90 by pressing the SHIFT and RESET ALL key; see table 3-2 for a list of default parameters. Press the ON/OFF key to turn on the output.
2. Connect the Model 90 and test equipment as shown in figure 3-4. Connect the Model 90 SYNC OUT to the scope's trigger input.

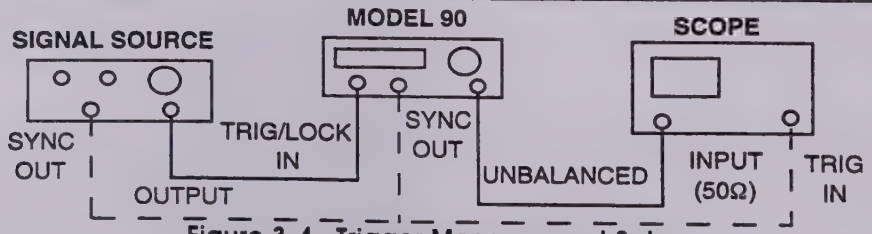


Figure 3-4. Trigger Measurement Setup

3. Set the Model 90 to the (Internal) Gate mode (MODE key). Internal gate is the default. Verify the scope displays an internally gated 5Vpp sine wave. Record (Record Yes or No) results on the form (Verification Form - Gate Mode Setting Internal Gated Sine Wave).

4. Set the Model 90 to the External Gate mode (TRIG/LOCK key). Set the signal source for a 100 Hz TTL square wave. Connect the signal source output to the TRIG/LOCK IN connector. Externally trigger the scope with the signal source output.

5. Verify the scope displays an externally gated 5Vpp sine wave. Record (Record Yes or No) the results on the form (Verification Form - Gate Mode Setting External Gated Sine Wave).

### Burst Mode

1. Initialize the Model 90 by pressing the SHIFT and RESET ALL key; see table 3-2 for a list of default parameters. Press the ON/OFF key to turn on the output.

2. Connect the Model 90 and test equipment as shown in figure 3-4. Connect the Model 90 SYNC OUT to the scope's trigger input.

3. Set the Model 90 to the (Internal) Burst mode (MODE key). Internal burst is the default. Verify the scope displays an internal triggered burst of 5, 5Vpp sine waves. Record (Record Yes or No) the results on the form (Verification Form - Burst Mode Setting Internal Burst Sine Wave).

4. Set the Model 90 to the external triggered burst mode (TRIG/LOCK key). Set the signal source for a 100 Hz TTL square wave. Connect the signal source to the TRIG/LOCK IN connector. Synchronize the scope off the signal source.

5. Verify the scope displays an externally triggered burst of 5, 5Vpp sine waves. Record (Record yes or No) the results on the form (Verification Form - Burst Mode Setting External Gated Sine Wave).

### Square Wave/Sync Out Transition Time

1. Initialize the Model 90 by pressing the SHIFT and RESET ALL key; see table 3-2 for a list of default parameters. Press the ON/OFF key to turn on the output.

2. Connect the Model 90 and test equipment as shown in figure 3-3. The Unbalanced Output must be terminated into a 50Ω feed-thru termination.

3. Set the Model 90 for 10 MHz square wave (FREQUENCY key and FUNCTION key). Measure rise time, fall time, positive-going transition peak-to-peak aberration in percent and negative-going transition peak-to-peak aberration in percent. Check the transition time and aberration as per the Specified Values, and record the results on the form (Verification Form - Square Wave/Sync Out Transition Time Unbalanced Output Setting Rise Time, Fall Time, Positive Transition % aberration, and Negative Transition Time % aberration).

4. Connect the Sync Out to the scope, and measure the peak-to-peak amplitude, rise time and fall time. Check the transition time as per the Specified Values, and record the results on the form (Verification Form - Square Wave/Sync Out Transition Time Sync Out Setting Rise Time and Fall Time).

### Outputs

1. Initialize the Model 90 by pressing the SHIFT and RESET ALL key; see table 3-2 for a list of default parameters. Press the ON/OFF key to turn on the output.

2. Connect the Model 90 and test equipment as shown in figure 3-3.

3. Set the Model 90 for 50Ω, 75Ω and 600Ω output impedance (SHIFT and SELECT key). The Unbalanced Output must be terminated into a matching feed-thru termination. Verify the scope displays the normal waveform and amplitude into matching terminations (Verification Form - Outputs Unbalanced Output Setting 50Ω, 75Ω, and 600Ω). Record (Record Yes or No) the results on the form.

4. Connect the Model 90 and test equipment as shown in figure 3-5.

5. Synchronize the scope off channel 1. Place a 135Ω load resistor across the Balanced Output terminals. Select the Model 90 135Ω Balanced Output (SHIFT and SELECT keys). Verify the scope displays on channel 1 and 2, two sine waves 180° out of phase. The amplitude of each sine wave will be one half of the Unbalanced Out sine wave (step 3). Record (Record Yes or No) the results on the form (Verification Form - Outputs Balanced Output Setting 135Ω).

6. Select the Balanced 600Ω Output. Place a 600Ω load resistor across the Balanced Output. Verify the scope displays on channel 1 and 2, two sine waves 180° out of phase. The amplitude of each sine wave will be one half of the Unbalanced Out

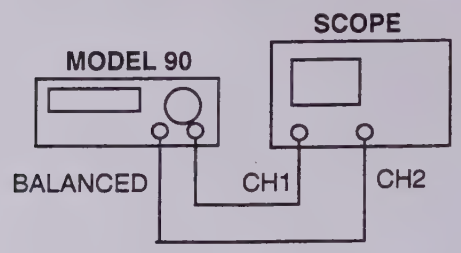



Figure 3-5. Balanced Output Verification

sine wave (step 3). Record (Record Yes or No) the results on the form (Verification Form - Outputs Balanced Output Setting 135Ω).

### Amplitude Modulation

1. Initialize the Model 90 by pressing the SHIFT and RESET ALL key; see table 3-2 for a list of default parameters. Press the ON/OFF key to turn on the output.
2. Connect the Model 90 and test equipment as shown in figure 3-6.
3. Set the signal generator for a 1kHz, 2.7 Vpp (open circuit) sine wave. Set Model 90 for 100 kHz (FREQUENCY key and knob/keypad) and the AM mode (MODE key). Verify the scope displays normal amplitude modulation of approximately 100%. Record (Record Yes or No) the results on the form (Verification Form - Amplitude Modulation Setting 100% AM).

### Suppressed Carrier

1. Initialize the Model 90 by pressing the SHIFT and RESET ALL key; see table 3-2 for a list of default parameters. Press the ON/OFF key to turn on the output.
2. Connect the Model 90 and test equipment as shown in figure 3-6.
3. Set Model 90 to the SCM mode (MODE key). With the MOD IN signal disconnected, verify the scope displays no output.
4. Set the signal source for +2Vdc. Connect the signal source output to the Model 90 MOD IN. Verify the scope displays a 4Vpp sine wave. Record (Record Yes or No) the results on the form (Verification Form - Suppressed Carrier Modulation Setting 4Vpp SCM).

### Sine Wave Purity

1. Initialize the Model 90 by pressing the SHIFT and RESET ALL key; see table 3-2 for a list of default parameters. Press the ON/OFF key to turn on the output.
2. Connect the Model 90 and test equipment as shown in figure 3-7.
3. Measure the sine total harmonic distortion in dB. Measure the sine wave purity, and Record the results on the form (Verification Form - Sine Wave Purity Setting THD at 1kHz).

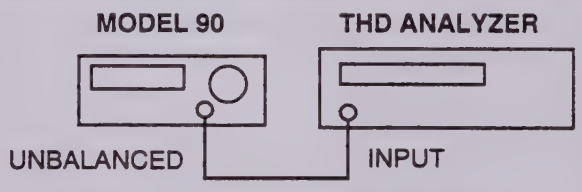



Figure 3-7. Sine Purity Measurement

### Amplitude Accuracy

1. Initialize the Model 90 by pressing the SHIFT and RESET ALL key; see table 3-2 for a list of default parameters. Press the ON/OFF key to turn on the output.
2. Connect the Model 90 and test equipment (DMM set to Vac) as shown in figure 3-8.
3. Set the amplitude as listed in the Verification Form - Amplitude Accuracy: Setting using the AMPLITUDE key and knob/keypad. Measure

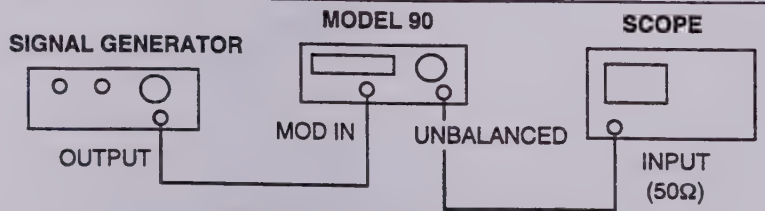



Figure 3-6. AM Verification

the amplitude accuracy per the Specified Value, and record the data on the form.

4. Set the Model 90 function to Triangle wave (FUNCTION key). Set the amplitude as listed in the Verification Form - Amplitude Accuracy Triangle Wave Setting using the AMPLITUDE key and knob/keypad. Measure the amplitude accuracy per the Specified Value, and record the data on the form.

5. Set the Model 90 function to Square wave (FUNCTION key). Set the amplitude as listed in the Verification Form - Amplitude Accuracy Square Wave Setting using the AMPLITUDE key and knob/keypad. Measure the amplitude accuracy per the Specified Value, and record the data on the form.

### DC Output and Attenuator Accuracy

1. Initialize the Model 90 by pressing the SHIFT and RESET ALL key; see table 3-2 for a list of default parameters. Press the ON/OFF key to turn on the output.

2. Connect the Model 90 and test equipment (DMM set to Vdc) as shown in figure 3-8.

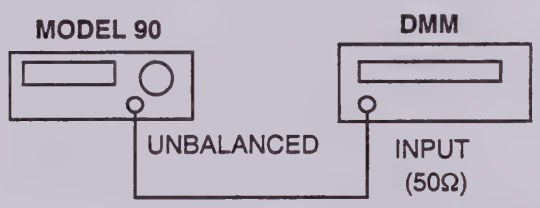



**Figure 3-8. Amplitude Accuracy**

3. Set the Model 90 to the DC function (FUNCTION key), and program the dc offsets (OFFSET key and keypad/knob) as listed in the Verification Form - DC Output and Attenuator Accuracy. Measure the dc offset accuracy as per the Specified Value. Record the data on the form.

### External Lock

1. Initialize the Model 90 by pressing the SHIFT and RESET ALL key; see table 3-2 for a list of default parameters. Press the ON/OFF key to turn on the output.

2. Connect the Model 90 and test equipment as shown in figure 3-9, except leave the signal source disconnected.

3. Set the Model 90 to external lock (TRIG/LOCK SOURCE key). Verify the Model 90 displays EXTLOC, the UNLOCK indicator flashes, and EXT indicator remains lit. Record (Record Yes or No) the results on the form (Verification Form - External Lock Setting Source Disconnected).

4. Set the signal source for a 10 kHz, 5Vpp sine wave. Connect the signal source to the Model 90 TRIG/LOCK IN connector. Verify the Model 90 displays EXTLOC 10.00 KHZ (approximate reading), UNLOCK indicator remains off, and the EXT indicator remains lit. Record (Record Yes or No) the results on the form (Verification Form - External Lock Setting Source Connected). The Model 90 automatically changes it frequency to match the frequency of the external source.

5. Set the Model 90 phase angle as per the "Setting". Measure the phase angle at each step. Measure the phase angle as per the Specified Value, and record results on the form.

### Front Panel

Did the annunciators and the display perform correctly during the Verification Procedure. Record the results

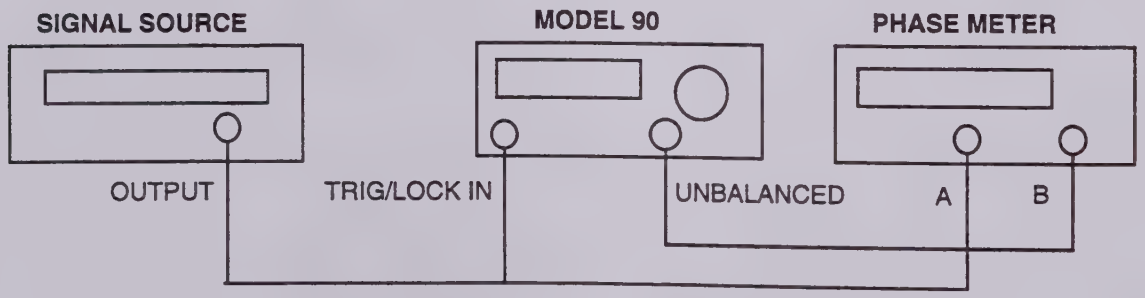



**Figure 3-9. External Lock Measurement**

on the form (Verification Form - Front Panel Display/ Annunciators.

Option 001 - High Frequency Stability Reference

Perform the following checks only if the Model 90 contains an Option 001.

1. Turn the Model 90 Power on.
2. Connect the Model 90 REF OUT, located on the rear panel, to a Counter/Timer.
3. Verify the REF OUT frequency measures within the Specified Value on the Verification Form. Record the results on the form.
5. Connect the Model 90 REF IN, located on the rear panel, to a signal source. Set the signal source to 10.001 MHz, 1Vrms sine wave (always properly terminate the signal source). Measure the REF OUT frequency as per the Specified Value, and record the results on the form.

| Parameter | Low Limit | High Limit |
|---|---|---|
| TCXO freq | 9,999,990 Hz | 10,000,010 Hz |
| 178 Freq | 10,000,000 Hz | 10,002,000 Hz |
| Ref Out | 178 Freq - 2 Hz | 178 Freq + 2 Hz |

## Option 002 - High Voltage Output

Perform the following checks only if the Model 90 contains an Option 002.

1. Initialize the Model 90 by pressing the SHIFT and RESET ALL key; see table 3-2 for a list of default parameters. Press the ON/OFF key to turn on the output.
2. Connect the Model 90 High Voltage Output, located on the rear panel, to the scope.
3. Select the Model 90 High Voltage Output by using the SHIFT and SELECT keys.
4. Set the Amplitude (AMPLITUDE key and keypad/ knob) as per "Setting" on the Verification Form. Observe the signal on the scope. Record the results on the form.

## VERIFICATION FORM

Date _____ Technician _____ Serial No _____

### Frequency Ranges

### Synthesized

| Settings | Data Record | Specified Value |
|---|---|---|
| 20 MHz | _____ MHz | 19.9998 to 20.0002 MHz |
| 2 MHz | _____ MHz | 1.99998 to 2.00002 MHz |
| 200 kHz | _____ kHz | 199.998 to 200.002 kHz |
| 20 kHz | _____ kHz | 19.9998 to 20.0002 kHz |
| 2 kHz | _____ kHz | 1.99998 to 2.00002 kHz |
| 200 Hz | _____ Hz | 199.998 to 200.002 Hz |
| 20 Hz | _____ Hz | 19.9998 to 20.0002 Hz |

### Unlocked FM

| Settings | Data Record | Specified Value |
|---|---|---|
| 20 MHz | _____ MHz | 19.4 to 20.6 MHz |
| 2 MHz | _____ MHz | 1.94 to 2.06 MHz |
| 200 kHz | _____ kHz | 194 to 206 kHz |
| 20 kHz | _____ kHz | 19.4 to 20.6 kHz |
| 2 kHz | _____ kHz | 1.94 to 2.06 kHz |
| 200 Hz | _____ Hz | 194 to 206 Hz |
| 20.00 Hz | _____ Hz | 19.4 to 20.6 Hz |

### Unlocked Continuous

| Settings | Data Record | Specified Value |
|---|---|---|
| 2.000 Hz | _____ Hz | 1.94 to 20.6 Hz |
| 200.0 mHz | _____ Hz | 194 to 206 mHz |
| 20.00 mHz | _____ mHz | 19.4 to 20.6 mHz |

### Frequency Resolution

| Settings | Data Record | Specified Value |
|---|---|---|
| 1999 Hz | _____ Hz | 1998.98 to 1999.02 Hz |
| 1888 Hz | _____ Hz | 1887.98 to 1888.02 Hz |
| 1777 Hz | _____ Hz | 1776.98 to 1777.02 Hz |
| 1666 Hz | _____ Hz | 1665.98 to 1666.02 Hz |
| 1555 Hz | _____ Hz | 1554.98 to 1555.02 Hz |
| 1444 Hz | _____ Hz | 1443.99 to 1444.01 Hz |
| 1333 Hz | _____ Hz | 1332.99 to 1333.01 Hz |
| 1222 Hz | _____ Hz | 1221.99 to 1222.01 Hz |
| 1111 Hz | _____ Hz | 1110.99 to 1111.01 Hz |
| 999 Hz | _____ Hz | 998.99 to 999.01 Hz |
| 888 Hz | _____ Hz | 887.991 to 888.009 Hz |
| 777 Hz | _____ Hz | 776.992 to 777.008 Hz |
| 666 Hz | _____ Hz | 665.993 to 666.007 Hz |
| 555 Hz | _____ Hz | 554.994 to 555.006 Hz |
| 444 Hz | _____ Hz | 443.996 to 333.003 Hz |
| 333 Hz | _____ Hz | 332.997 to 333.003 Hz |
| 222 Hz | _____ Hz | 221.998 to 222.002 Hz |

## VERIFICATION FORM (Continued)

### Symmetry

| Settings | Data Record | Specified Value |
|---|---|---|
| 10% Symmetry | _____ µs | 99 to 101 µs |
| 20% Symmetry | _____ µs | 198 to 202 µs |
| 30% Symmetry | _____ µs | 297 to 303 µs |
| 40% Symmetry | _____ µs | 396 to 404 µs |
| 50% Symmetry | _____ µs | 495 to 505 µs |
| 60% Symmetry | _____ µs | 594 to 606 µs |
| 70% Symmetry | _____ µs | 693 to 707 µs |
| 80% Symmetry | _____ µs | 792 to 808 µs |
| 90% Symmetry | _____ µs | 891 to 908 µs |

### VCF/FM

| Setting | Data Record | Specified Value |
|---|---|---|
| Center Frequency | _____ Hz | 970 to 1030 Hz |
| Deviation Frequency | _____ Hz | 1900 to 2100 Hz |

### Waveforms

| Setting | Data Record | Specified Value |
|---|---|---|
| Sine Wave | _____ | Record: Yes or No |
| Triangle Wave | _____ | Record: Yes or No |
| Square Wave | _____ | Record: Yes or No |
| DC | _____ | Record: Yes or No |

### Sweep

| Setting | Data Record | Specified Value |
|---|---|---|
| Sweep Output | _____ | Record: Yes or No |
| Sweep Ramp | _____ | Record: Yes or No |

### Continuous Mode

| Setting | Data Record | Specified Value |
|---|---|---|
| Continuous 5Vpp Sine | _____. | Record: Yes or No |

### Triggered Mode

| Setting | Data Record | Specified Value |
|---|---|---|
| Internal Triggered Sine Wave | _____ | Record: Yes or No |
| External Triggered Sine Wave | _____ | Record: Yes or No |

### Gate Mode

| Setting | Data Record | Specified Value |
|---|---|---|
| Internal Gated Sine Wave | _____ | Record: Yes or No |

### Gate Mode

| Setting | Data Record | Specified Value |
|---|---|---|
| External Gated Sine Wave | _____ | Record: Yes or No |

### Burst Mode

| Setting | Data Record | Specified Value |
|---|---|---|
| Internal Burst Sine Wave | _____ | Record: Yes or No |
| External Burst Sine Wave | _____ | Record: Yes or No |

## VERIFICATION FORM (Continued)
## Square Wave/Sync Out Transition Time

### Unbalanced Output

| Setting | Data Record | | Specified Value |
|---|---|---|---|
| Rise Time | _____ | ns | < 9ns |
| Fall Time | _____ | ns | < 9 ns |
| Pos. Trans. % aberration | _____ | % | < 5.2% |
| Neg. Trans. % aberration | _____ | % | < 5.2% |

### Sync Out

| Setting | Data Record | | Specified Value |
|---|---|---|---|
| Rise Time | _____ | ns | < 11 ns |
| Fall Time | _____ | ns | < 11 ns |

### Outputs

### Unbalanced Output

| Setting | Data Record | Specified Value |
|---|---|---|
| 50Ω (5Vpp Sine Wave) | _____ | Record: Yes or No |
| 75Ω (5Vpp Sine Wave) | _____ | Record: Yes or No |
| 600Ω (5Vpp Sine Wave | _____ | Record: Yes or No |

### Balanced Output

| Setting | Data Record | Specified Value |
|---|---|---|
| 135Ω (180°, 5Vpp Sine Wave) | _____ | Record: Yes or No |
| 600Ω (180°, 5Vpp Sine Wave) | _____ | Record: Yes or No |

### Amplitude Modulation

| Setting | Data Record | Specified Value |
|---|---|---|
| ≈100% AM | _____ | Record: Yes or No |

### Suppressed Carrier Modulation

| Setting | Data Record | Specified Value |
|---|---|---|
| ≈4.8 Vp SCM | _____ | Record: Yes or No |

### Sine Wave Purity

| Setting | Data Record | | Specified Value |
|---|---|---|---|
| THD at 1 kHz | _____ | dB | ≤ – 46 dB (0.5%) |

### Amplitude Accuracy

### Sine Wave

| Setting | Data Record | | Specified Value |
|---|---|---|---|
| 1.11 Vpp | _____ | Vrms | 0.38105 to 0.40375 Vrms |
| 2.22 Vpp | _____ | Vrms | 0.7657 to 0.8041 Vrms |
| 3.33 Vpp | _____ | Vrms | 1.14996 to 1.20404 Vrms |
| 4.44 Vpp | _____ | Vrms | 1.5351 to 1.6049 Vrms |
| 5.55 Vpp | _____ | Vrms | 1.91926 to 2.00474 Vrms |
| 6.66 Vpp | _____ | Vrms | 2.3044 to 2.4056 Vrms |
| 7.77 Vpp | _____ | Vrms | 2.68856 to 2.80544 Vrms |
| 8.88 Vpp | _____ | Vrms | 3.07370 to 3.20630 Vrms |
| 9.99 Vpp | _____ | Vrms | 3.45786 to 3.60614 Vrms |
| 15.0 Vpp | _____ | Vrms | 5.19344 to 5.41256 Vrms |

## VERIFICATION FORM (Continued)

### Triangle Wave

| Setting | Data Record | Specified Value |
|---|---|---|
| 1.11 Vpp | _____ Vrms | 0.31109 to 0.32971 Vrms |
| 2.22 Vpp | _____ Vrms | 0.62518 to 0.65662 Vrms |
| 3.33 Vpp | _____ Vrms | 0.93917 to 0.98343 Vrms |
| 4.44 Vpp | _____ Vrms | 1.25346 to 1.31054 Vrms |
| 5.55 Vpp | _____ Vrms | 1.56706 to 163694 Vrms |
| 6.66 Vpp | _____ Vrms | 1.88164 to 1.96436 Vrms |
| 7.77 Vpp | _____ Vrms | 2.19524 to 2.29076 Vrms |
| 8.88 Vpp | _____ Vrms | 2.50884 to 2.61716 Vrms |
| 9.99 Vpp | _____ Vrms | 2.82342 to 2.94458 Vrms |
| 15.0 Vpp | _____ Vrms | 4.24050 to 4.41950 Vrms |

### Square Wave

| Setting | Data Record | Specified Value |
|---|---|---|
| 1.11 Vpp Square | _____ Vrms | 0.53890 to 0.57110 Vrms |
| 2.22 Vpp Square | _____ Vrms | 1.08280 to 1.13720 Vrms |
| 3.33 Vpp Square | _____ Vrms | 1.62670 to 1.70330 Vrms |
| 4.44 Vpp Square | _____ Vrms | 2.17060 to 2.26940 Vrms |
| 5.55 Vpp Square | _____ Vrms | 2.71450 to 2.83550 Vrms |
| 6.66 Vpp Square | _____ Vrms | 3.25840 to 3.40160 Vrms |
| 7.77 Vpp Square | _____ Vrms | 3.80230 to 3.96770 Vrms |
| 8.88 Vpp Square | _____ Vrms | 4.34620 to 4.53380 Vrms |
| 9.99 Vpp Square | _____ Vrms | 4.89010 to 5.09990 Vrms |
| 15.0 Vpp Square | _____ Vrms | 7.34500 to 7.65500 Vrms |

### DC Output/Attenuator Accuracy

| Setting | Data Record | Specified Value |
|---|---|---|
| +7.499V | _____.Vdc | +7.415 to +7.585 Vdc |
| 0V | _____ Vdc | -0.001 to +0.001 Vdc |
| -7.499V | _____ Vdc | -7.585 to -7.415 Vdc |

### External Lock

| Setting | Data Record | Specified Value |
|---|---|---|
| Source Disconnected | _____ | Record: Yes or No |
| Source Connected | _____ | Record: Yes or No |

### Phase Angle

| Setting | Data Record | Specified Value |
|---|---|---|
| 0° Phase | _____ ° | –4° to +4° |
| +90° Phase | _____ ° | +86° to +94° |
| +180° Phase | _____ ° | +176° to +184° |
| –90° Phase | _____ ° | –94° to –86° |
| –180° Phase | _____ ° | –184° to –176° |

## VERIFICATION FORM (Continued)

### Front Panel

| | Data Record | Specified Value |
|---|---|---|
| Display/Annunciators | _____ | Record: Yes or No |

### High Voltage Output Option

| Settings | Data Record | Specified Value |
|---|---|---|
| 40 Vpp Sine Wave | _____ | 38.79 to 41.21 Vpp |
| 30 Vpp Sine Wave | _____ | 29.09 to 30.91 Vpp |
| 10 Vpp Sine Wave | _____ | 9.69 to 10.31 Vpp |
| 5Vpp Sine Wave | _____ | 4.85 to 5.15 Vpp |
| 100 mVpp Sine Wave | _____ | 96 to 104 mVpp |

## 4.1 CALIBRATION

Wavetek maintains a factory Customer Service department for those customers not possessing the necessary personnel or test equipment to calibrate or repair the instrument. Before returning the instrument, contact the Customer Service Department by calling or writing:

Wavetek San Diego, Inc.
9045 Balboa Ave.
San Diego, CA 92123
Telephone: (619) 279-2200
TWX: (910) 335-2007
FAX (619) 565-9558

The Model 90 provides the user with two calibration methods: Autocal and Calibrate.

### 4.1.1 Autocal

Autocal (automatic calibration) provides a quick method of calibrating the Model 90 without using external test equipment. Autocal automatically sets up the instrument and takes internal measurements using internal standards. The Model 90 calculates correction values and stores those values in memory. These correction values are recalled from memory when the unit is powered up. Use Autocal when Model 90 accuracy is critical, after long term instrument storage, following drastic changes in the environment, or when the operator believes Autocal is necessary.

### 4.1.2. Calibration Procedure

The calibration provides a more extensive method of calibration. The Calibration Procedure uses external test equipment and requires opening the instrument and making adjustments. Use the Calibration Procedure when the Model 90 displays "CAL REQUIRED" or "FAILED AUTO CAL", when the Model 90 has been repaired, fails the Performance Verification procedure (Appendix A), or when routine calibration is scheduled. Paragraph 4.3 describes the Calibrate procedure.

## 4.2 AUTO CAL PROCEDURE

To Auto Cal the Model 90, perform the following steps. Auto Cal requires no external test equipment. In fact, no test equipment can be connected to the input connectors otherwise the Auto Cal circuitry could alter the calibration of the instrument. Also, disconnect all outputs from the instrument otherwise the sudden changes in the instrument's output waveforms could damage external equipment.

1. Turn on the Model 90 and allow it to warm up for 20 minutes. Pressing the CALIBRATE key during the 20 minute warm up time displays the countdown time, after the 20 minutes the Model 90 begins Auto Cal. Pressing any other key during the count down aborts Auto Cal and returns the instrument to normal operation.

   Remember to remove all input and output connections to the Model 90 before pressing Auto Cal.

2. If the unit has been on for more than 20 minutes, press the CALIBRATE key (SHIFT and CALIBRATE) and allow the unit time to complete the Auto Cal cycle. While running Autocal, the Model 90 displays "CALIBRATING". When completed successfully, the Model 90 displays "AUTOCALIBRATED" and the unit returns to its last setting. If the Auto Cal fails, the Model 90 displays an error message which identifies the parameter - ERR (*Keyword*); for example ERR VSINCAL. If this occurs occasionally, try to Calibrate the unit again. Note the error keywords and report the errors when the unit is returned for scheduled maintenance. Refer to paragraph 6.7.6 for a listing of error messages.

3. If the unit displays AUTOCAL DISABLED, the Calibration Technician disabled Autocal during the calibration procedure to keep unauthorized personnel performing Autocal.

## 4.3 CALIBRATION PROCEDURE

To perform the complete manual calibration procedure follow the steps listed below. This procedure contains a series of steps which the Model 90 guides you through. During this procedure, the Model 90 automatically sets itself to the right conditions. Some calibration steps may require you to make changes using front panel controls.

**Table 4-1. Recommended Test Equipment**

| Test Equipment | Recommended Model |
|---|---|
| Scope | Tektronix 2465 or equivalent. |
| Distortion Analyzer | Hewlett Packard 8903B or equivalent. |
| Digital Voltmeter | Wavetek Model 1062 or equivalent. |
| Function Generator | Wavetek Model 23 or equivalent. |
| Frequency Counter | Hewlett Packard 5335A or equivalent. |
| Phase Meter | Hewlett Packard 3575A or equivalent. |

*NOTE*

*Use rear panel for all ground connections unless otherwise specified.*

*All indications and waveforms are referenced to chassis ground unless otherwise specified.*

### Adjustments

Throughout this procedure are illustrations identifying the adjustments used in the steps. For a detailed look at the adjustment locations, refer to the assembly drawings located in section 7 of this manual. Figure 4-1 shows the individual board locations.

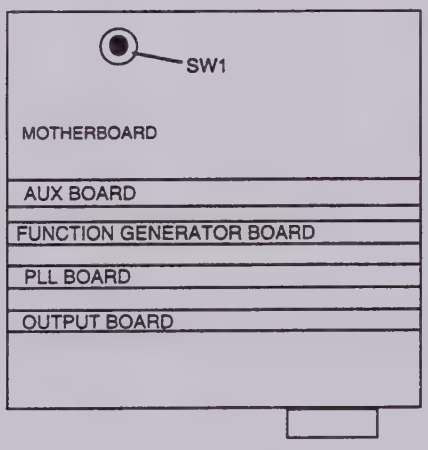



**Figure 4-1. Board Locator**

### Keys

While performing the Calibration Procedure, the following keys perform the following functions.

| | |
|---|---|
| CALIBRATE | Pressing this key during the Calibration Procedure will turn off the Calibration mode. |
| RESET | During the Calibration Procedure, this key resets all the calibration factors to their default values. |
| ⇒ CURSOR | During the Calibration Procedure, this key functions as the forward cursor. Pressing the ⇒ CURSOR key advances the procedure to the next calibration step. |
| ⇐ CURSOR | During the Calibration Procedure, this key functions as the reverse cursor. Pressing the ⇐ CURSOR key backs the procedure up to the previous calibration step. |
| KNOB | During the Calibration Procedure, the KNOB is used to change and enter calibration data. It is also used to alternate between two functions in some steps. |
| KEYPAD | During the Calibration Procedure, the numeric keypad is used to enter calibration data. |
| ENTER | Use the ENTER key to accept data entered using the numeric keypad. |

### Precalibration Setup

Before beginning calibration, disconnect the Model 90 from its power source and remove five top cover screws. Slide the top cover off, and remove the inner shield. Slide the top cover back on.

*NOTE*

*Keep the top cover in place during the procedures except when necessary to make an internal adjustment.*

2. Perform the turn-on procedures as described in paragraph 2.4.3 of the Model 90 Operator's Manual.

**WARNING**

**Dangerous voltages are present with the covers removed. Where maintenance can be performed without power applied, the power should be removed. Battery voltage is present even with AC power cable removed.**

3. Connect the Model 90 to the power source, turn the power on, and allow the unit to warm up for 20 minutes.

**Step 1 Adjust Frequency Reference**

If calibrating a standard Model 90 (one without Option 001, TCXO Frequency Reference) perform items 1 through 4 of this step. If Option 001 is installed perform items 1, 5, and 6.

1. After warm up, reset the Model 90 by pressing the Model 90 SHIFT and RESET ALL keys.
2. Connect the test equipment as shown in figure 4-2.
3. Set up the Model 90 for a 1MHz output by pressing the FREQUENCY, 1E6, and ENTER keys. Press ON/OFF to turn on the output.
4. Measure the frequency at the Sync Out connector. Verify the counter reads 1MHz ±5Hz. If incorrect, slide the cover back, adjust C150 (see figure 4-3) until the counter reads 1MHz ±5Hz, and then slide the cover back on.

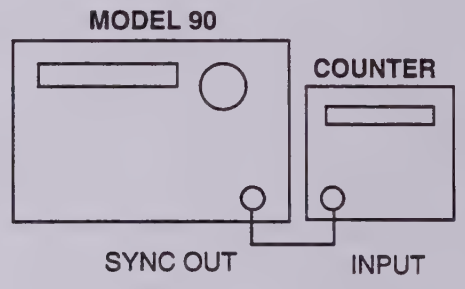



**Figure 4-2. Frequency Reference Setup**

If the Option 001, TCXO Frequency Reference is installed, perform item 1 of this step and continue on using the following steps.

5. Connect the counter/timer to the Model 90 REF OUT connector, located on the rear panel.
6. Measure the frequency at the REF OUT connector. Verify the counter reads 10 MHz ±2Hz.

   If incorrect, turn off the Model 90 and slide the cover back. Place the Auxiliary board on an extender card. Turn the power back on. Remove the sticker from the TCXO and adjust the trimmer (see figure 4-3) until the counter reads 10 MHz ±2Hz.

   When finished, turn off the power, replace the sticker on the TCXO, remove the extender card, and place the Auxiliary board back in the unit. Slide the cover on. Then turn on the power.

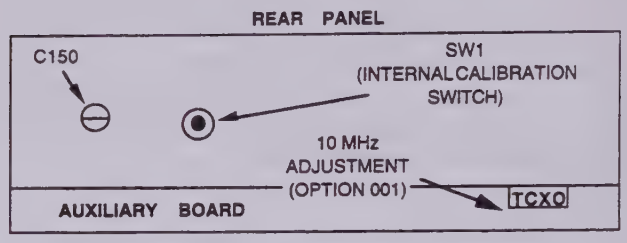



**Figure 4-3. Frequency Reference/TCXO Locator**

**Step 2 Initial Steps**

1. After the unit is warmed up (20 minutes) slide the top cover back. Press and hold down the internal calibration switch SW1 (figure 4-3) while pressing the SHIFT and CALIBRATE keys. Slide the cover back on.
2. Verify the Model 90 display indicates WVTK SN XXXXXXX or WVTK SN 0. Press the front panel ⇒ CURSOR key to step to USER SN XXXX.
3. Verify the Model 90 display flashes CALIBRATING and then indicates USER SN XXXX or USER SN 0. USER SN allows the calibrator to enter an identification number using the knob or keypad. Press the ⇒ CURSOR key to advance to R33,97, VSINE XXX. Pressing the ⇒ CURSOR key also stores the User Number.

**Step 3. Adjust Sine Wave.**

1. The Model 90 displays R33, 97, VSINE XXX where XXX represents the internal programmed value of the VSINE dc control voltage. Connect the test equipment as shown in figure 4-4.
2. Set the distortion analyzer controls to display the Model 90 output signal Total Harmonic Distortion (THD) in dB.

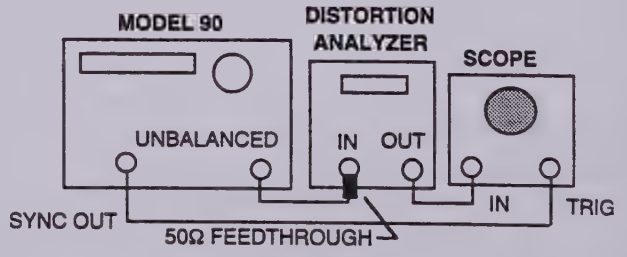



**Figure 4-4. Sine Wave Adjust Setup**

3. On the Model 90, slowly adjust the Knob for minimum THD as displayed on the scope. Verify that reading is ≤ – 50 dB at 10 kHz.

4. If incorrect, set the scope controls to display the distortion analyzer output. Slide the cover back. Adjust R33 (figure 4-5) until waveform peaks are clearly visible in the residue.

   Adjust R97 (figure 4-5) until waveform peaks are symmetrical, one above the average value of the residue signal and one below.

**Figure 4-5. R33/R97 Locator**

5. Adjust R33 until the peaks disappear back into the residue.

6. Observe the overall ripple in the residue displayed on the scope. Turn the Model 90 Knob CW until the waveform peaks are clearly visible in the residue and repeat step 5.

   If the overall ripple has decreased, continue the procedure always turning the Model 90 Knob CW.

   If the overall ripple has increased, continue the procedure always turning the Model 90 Knob CCW.

7. Repeat steps 5 and 6 until:

   The amplitude of the overall ripple in the residue signal is minimum as displayed on the scope. The THD as measured on the distortion analyzer is ≤-50 dB.

8. Disconnect the test equipment and slide the cover back on.

9. On the Model 90, press the ⇒ CURSOR key to advance to the next step. Verify the display flashes CALIBRATING and then indicates SCM NULL -XXX.

#### Step 4. SCM Null

1. The Model 90 displays SCM NULL -XXX where -XXX represent the SCM null value.

2. Connect the test equipment as shown in figure 4-7. Set the scope for 50 mV/div (Vdc).

3. View the carrier null signal on the scope. If necessary, slide the cover back and adjust R146 (see figure 4-6) to center the display. Then use the knob to adjust for best square wave signal null. Slide the top cover back on.

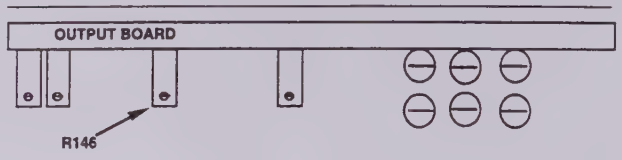



**Figure 4-6. R146 Locator**

4. Press the ⇒ CURSOR key to step to TRI NULL R25 2.

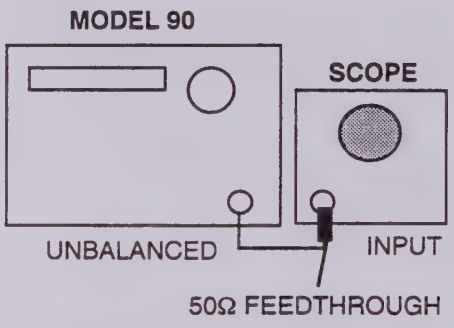



**Figure 4-7. SCM Null Setup**

#### Step 5 Null Triangle

1. The Model 90 displays TRI NULL R25 2. Connect test equipment (DVM set to Vdc) as shown in figure 4-8.

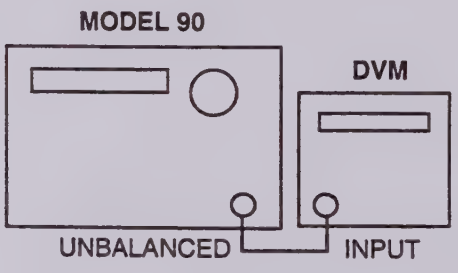



**Figure 4-8. Triangle Null Setup**

2. The DVM measures the dc offset value of the 2Vpp triangle.

3. Rotate the knob on the Model 90 until display shows TRI NULL R25 15. The DVM measures the dc offset value of the 15 Vpp triangle.

4. Use the knob to move between "2" and "15". Slide the cover back, and adjust the Output board's R25 (see figure 4-9) until the dc offset change be-

tween 2 and 15 is less than 2mV at both amplitudes. Slide the cover back on.

5. Press the ⇒ CURSOR key to advance to the next step. Verify the display flashes CALIBRATING and then indicates TRI OFFSET R146.

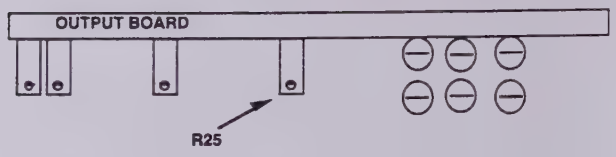



Figure 4-9. R25 Locator

**Step 6 Adjust Triangle Offset**

1. The Model 90 displays TRI OFFSET R146. Leave the test equipment connected as shown in figure 4-8.
2. Slide the cover back, and adjust the Output board's R146 (see figure 4-10) until the DVM reads 0Vdc ±2mVdc of triangle offset. Slide the cover back on.
3. Press the ⇒ CURSOR key to advance to the next step. Verify the display flashes CALIBRATING then indicates SINE NULL R64.

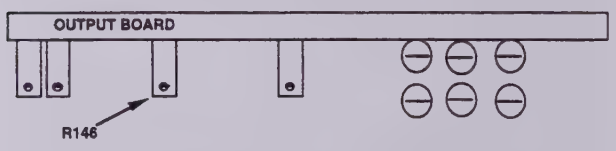



Figure 4-10. R146 Locator

**Step 7 Null Sine Wave**

1. The Model 90 displays SINE NULL R64. Leave the test equipment connected as shown in figure 4-8.
2. Slide the cover back, and adjust the PLL board's R64 (see figure 4-11) until the DVM reads 0Vdc ±2mVdc of sine offset. Slide the cover back on.
3. On the Model 90, press the ⇒ CURSOR key to advance to the next step. Verify the display flashes CALIBRATING and then indicates SQUARE 0 R158.

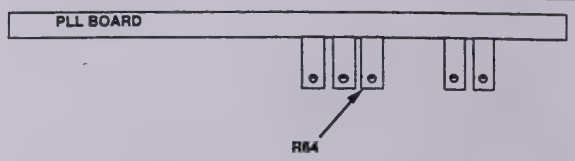



Figure 4-11. R64 Locator

**Step 8 Null Square**

1. The Model 90 displays SQUARE 0 R158. Leave the test equipment connected as shown in figure 4-8.
2. Slide the cover back, and adjust the Output board's R158 (see figure 4-12) until the DVM reads 0Vdc ±2mVdc of square offset. Slide the cover back on.
3. Press the ⇒ CURSOR key to advance to the next step. Verify the display flashes CALIBRATING then indicates TRI AMPL R211 1.

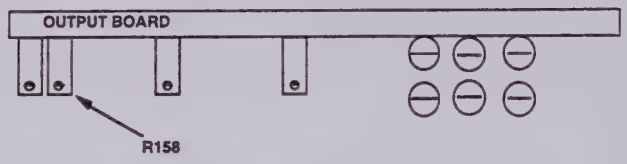



Figure 4-12. R158 Locator

**Step 8 Adjust Triangle Amplitude**

1. The Model 90 displays TRI AMPL R211 1. Connect test equipment (Scope set for Vdc) as shown in figure 4-13. Note the amplitude of the triangle wave.

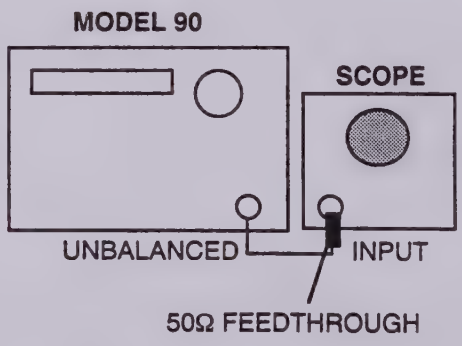



Figure 4-13. Triangle Amplitude Setup

2. On the Model 90, rotate the knob until display shows TRI AMPL R211 2. Note the amplitude of the square wave.
3. Use the knob to step between the triangle and square waves. Slide the cover back. Adjust R211 on the PLL board until the peak to peak amplitude of the triangle matches the peak to peak amplitude of the square wave. See figure 4-14. Slide the cover back on.

4. Press the ⇒ CURSOR key to advance to the next step. Verify the display flashes CALIBRATING then indicates SIN AMPL R208 0.

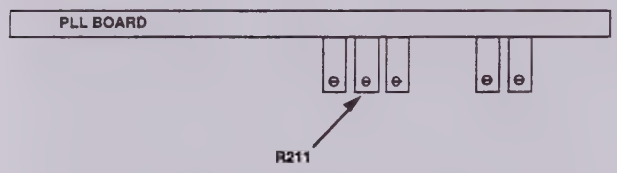



Figure 4-14. R211 Locator

**Step 10 Adjust Sine Amplitude**

1. The Model 90 displays SIN AMPL R208 0. Leave the test equipment connected as shown in figure 4-13.
2. On the Model 90, rotate the knob until display shows SIN AMPL R208 2. Note the amplitude of the square wave.
3. Use the knob to step between the sine and square waves. Slide the cover back. Adjust R208 on the PLL board (see figure 4-15) until the peak to peak amplitude of the sine wave matches the peak to peak amplitude of the square wave. Slide the cover back on.
4. Press the ⇒ CURSOR key to advance to the next step. Verify the display flashes CALIBRATING then indicates HF SYM R9.

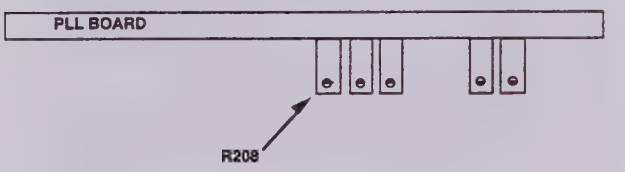



Figure 4-15. R208 Locator

**Step 11 Adjust High Frequency Symmetry**

1. The Model 90 displays H F SYM R9. Leave the test equipment connected as shown in figure 4-13.
2. Slide the cover back, and adjust R9 on the output board (see figure 4-16) while observing the scope. Use the scopes delta time cursors to measure the two halves of the square's time symmetry between the 50% points. Adjust R9 until the time symmetry is equal ±0.5 ns. Slide the cover back on.
3. Press the fi CURSOR key to advance to the next step. Verify the display flashes CALIBRATING then indicates H F QUAL R69, ..., R86.

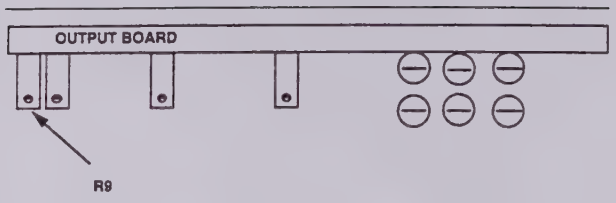



Figure 4-16. R9 Locator

**Step 12 Adjust High Frequency Waveform Quality**

1. The Model 90 displays H F QUAL R69, ... , R86. Leave test equipment as shown in figure 4-13.
2. Slide the cover back. Adjust R69, R70, R67, R86, R84, and R87 on the output board (see figure 4-17) for best time symmetry and aberrations. The leading and trailing edge transition time must be less than 7.5ns. Transition time is measured between the 10% and 90% points of the square wave. Aberration must be less than 4%. The Model 90 unbalanced output must be terminated with 3 feet of coax cable and the cable terminated with a 50Ω terminator for specified waveform quality. Slide the cover back on.
3. Press the ⇒ CURSOR key to advance to the next step. Verify the display flashes CALIBRATING then indicates PHASE 0 XXXXX.

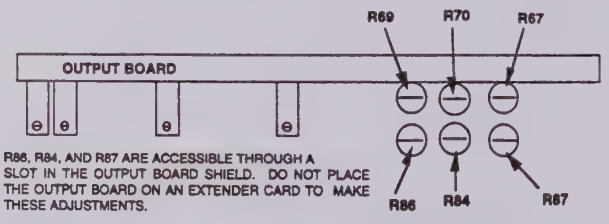

R69
R70
R67
OUTPUT BOARD
R86, R84, AND R87 ARE ACCESSIBLE THROUGH A SLOT IN THE OUTPUT BOARD SHIELD. DO NOT PLACE THE OUTPUT BOARD ON AN EXTENDER CARD TO MAKE THESE ADJUSTMENTS.
R86
R84
R87

Figure 4-17. R69, R70, R86, R87, R84, and R67 Locator

**Step 13 Adjust Phase 0°**

1. The Model 90 displays PHASE0Y XXXXX where XXXXX represents a calibration value. Connect the test equipment as shown in figure 4-18. Appendix B contains an alternate method of calibrating phase using a scope.
2. Set the signal source controls as follows:
   Set Function to Sine.
   Frequency to 2.01 kHz.
   Output Level to 5Vpp.

3. On the Model 90,

   Adjust the Knob to until the phase meter read 0°.

   Press the ⇒ CURSOR key. Verify that the display flashes CALIBRATING for then displays PHASE+180Y XXXXX. Pressing ⇒ CURSOR key stores the calibration value in internal memory.

**Step 14 Adjust Phase +180°**

1. The Model 90 displays PHASE+180Y XXXXX where XXXXX represents a calibration value. Leave the test equipment connected as shown in figure 4-18. Do not change the signal source. Appendix B contains an alternate method of calibrating phase using a scope.
2. On the Model 90,

   Adjust the Knob to until the phase meter reads +180°.

   Press the ⇒ CURSOR key advance to the next step. Verify the display flashes CALIBRATING and then displays PHASE–180Y XXXXX. Pressing ⇒ CURSOR key stores the calibration value in internal memory.

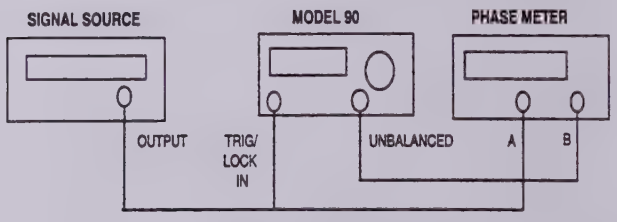



**Figure 4-18. Phase Setup**

**Step 15 Adjust Phase -180°**

1. The Model 90 displays PHASE-180Y XXXXX where XXXXX represents a calibration value. Leave the test equipment connected as shown in figure 4-18. Do not change the signal source. Appendix B contains an alternate method of calibrating phase using a scope.
2. On the Model 90,

   Adjust the Knob to until the phase meter reads -180°

   Press ⇒ CURSOR key to advance to the next step. Verify that the display flashes CALIBRATING and then displays SQ PHASE 0 XXXXX. Pressing ⇒ CURSOR key stores the calibration value in internal memory.

**Step 16 Adjust Square Phase 0°**

1. The Model 90 displays SQ PHASE 0 XXXXX where XXXXX represents a calibration value. Leave the test equipment connected as shown in figure 4-18. Do not change the signal source. Appendix B contains an alternate method of calibrating phase using a scope.
3. On the Model 90,

   Adjust the Knob until the phase meter reads 0°.

   Press the ⇒ CURSOR key to advance to the next step. Verify the display flashes CALIBRATING and then displays CONFIDENCE. Pressing ⇒ CURSOR key stores the calibration value in internal memory.

**Step 17 (Option 002 Only) High Voltage Option Waveform Quality**

If Option 002 is not installed, this Calibration item will not appear.

1. The Model 90 displays HVQ C28, R32, R33. Connect test equipment as shown in figure 4-19.

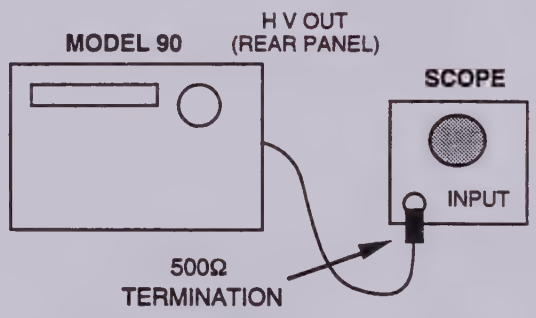



**Figure 4-19. High Voltage Output Setup**

2. On the Model 90, adjust C28, R32, and R33 on the Auxiliary board (see figure 4-20) for leading and trailing edge transition times of less than 140 ns. Transition time is measured between the 10% and 90% points of the square wave. The square wave should appear overdamped with no aberrations.

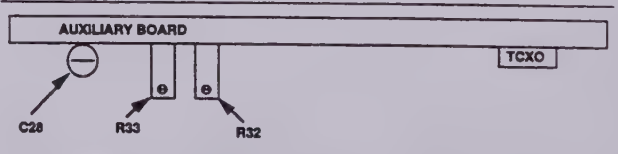



**Figure 4-20. High Voltage Option Locator**

3. On the Model 90, press the ⇒ CURSOR key to advance to the next step. Verify the display flashes CALIBRATING and then displays CONFIDENCE.

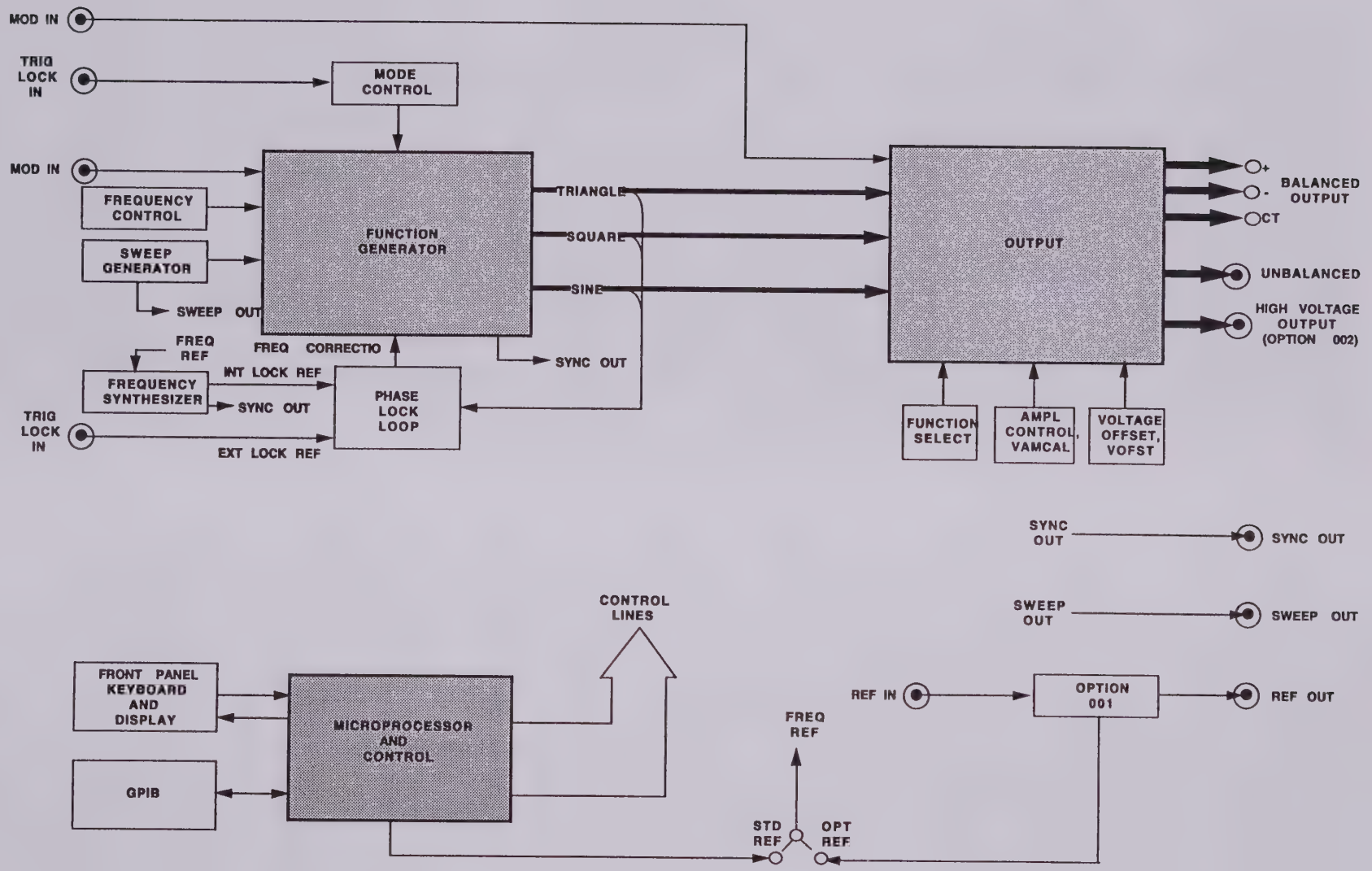



Figure 5-1. Model 90 Functional Block Diagram

## 5.1 The Model 90

This section describes the Model 90 Synthesized Function Generator. Section 5 is divided into two parts: the basic functional block description and the detailed block descriptions. The intent is to provide an insight into signal flow through the Model 90, as well as, what controls that signal flow.

In this description, functional blocks are organized by signal flow rather than actual assemblies. The Model 90 consists of three major functional blocks (Function Generator, Output, and Microprocessor Section) as shown in figure 5-1. The waveforms originate from the Function Generator and is routed to the Output block. All functional blocks are contained in six separate assemblies (Motherboard, Output board, Function Generator board, Phase Lock Loop board, Aux board, and Front Panel). The motherboard links all blocks within the Model 90.

The Function Generator block produces the triangle, square and sine waves supplied by the Model 90. Also, it provides frequency and symmetry control of the waveforms. Frequency of the Function Generator is controlled by one of four inputs: Frequency Control, Sweep Generator, and Phase Lock Loop, plus external Modulation Input.

Frequency Control sets up the generator's fixed frequency. If a synthesizer mode is selected, the Phase Lock Loop supplies a frequency correction voltage which locks the Function Generator's frequency to an internal or external frequency. The Phase Lock Loop receives its internal frequency input from the Frequency Synthesizer which is referenced to the Freq Ref or optional reference. The phase lock loop gets its external frequency from Trig Lock In connector which allows phase shift of the output waveform relative to the source. If the sweep mode is selected, the Sweep Generator sets the stop frequency and sweep length; Frequency Control sets the start frequency. Another frequency control input, Mod In, allows external modulation of the frequency.

The Mode Control controls the operating mode of the Function Generator. It allows the Function Generator to produce continuous waveforms, single cycled triggered waveforms, and multiple cycled gated and burst waveforms. Burst allows a user-defined number of cycles to be produced.

The Output block selects the waveform, controls the output level and offset, and drives the external devices. The output level can be fixed or modulated (Amplitude Modulated or Suppressed Carrier Modulated). An optional High Voltage Output permits output between 1mVpp and 40 Vpp of all functions and modes.

The Microprocessor Section provides the processing and interfacing for the Model 90. It supplies the analog control voltages like the frequency control voltage or amplitude control voltage. It also supplies the digital control line that control the signal routing through out the Model 90. The Microprocessor Section interfaces with the display/keyboard and the GPIB interface.

## 5.2 Function Generator

### 5.2.1 Introduction

The function generator section produces the square and triangle waves of the Model 90, as well as, the sine wave. The Function Generator block includes:

VCG Summing Amplifier,

Symmetry Control,

Function Generator Loop (current sources, frequency range capacitors, capacitance multiplier, triangle buffer, comparator, and diode gates)

High Frequency Compensation,

Sine Convertor,

Trigger (Mode) Control.

Figure 5-2 illustrates the Function Generator Block. The heavy lines through the diagram indicates signal flow.

The Phase Lock Loop, Frequency Control, Sweep Generator, and Mod In provide either dc or AC plus dc voltage to the VCG Summing amplifier. These inputs control the instantaneous frequency of the waveform. The

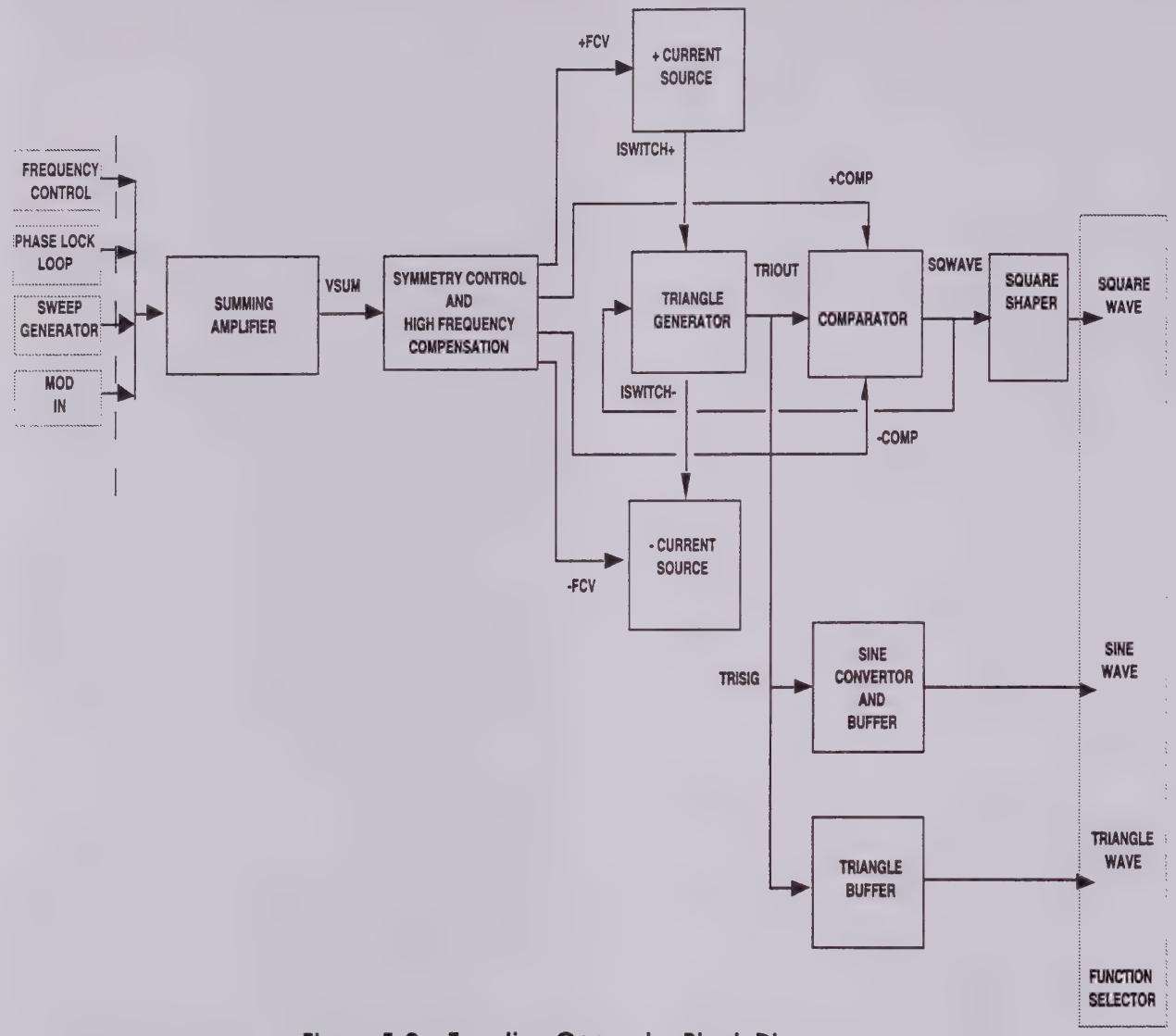



**Figure 5-2. Function Generator Block Diagram**

VCG Summing Amplifier produces an output , VSUM, which is the summation of all four inputs. VSUM drives the Symmetry control which produces two voltages, +FCV and –FCV, which will control the VCG (constant) Current Sources. When the waveform symmetry is 50%, the two voltages, +FCV and -FCV, will be equal but opposite polarity. However when the symmetry is anything but 50%, the voltages, +FCV and -FCV will be unequal. The VCG Current Sources controls the charge and discharge rate of the Function Generator Loop's Frequency Range Capacitors. The Function Generator Loop produces two output signals: the square wave and the triangle wave. The square wave runs directly to the Square Shaper (paragraph 5.3.2). The triangle wave drives the Triangle Buffer or the Sine Convertor. The outputs from the Sine Converter and Triangle Buffer drive the Function Selector (paragraph 5.3.2). The High Frequency Compensation circuit makes allowances for delays in the Function Generator Loop at the higher frequencies. Trigger Control turns on or off the Function Generator Loop based on the mode selected.

### 5.2.2 Function Generator Loop

The Function Generator Loop consists of the VCG Current Sources, Frequency Range Capacitors, Capacitance

Multiplier, Triangle Buffer, Comparator, and Diode Gates. The Function Generator Loop produces the unit's square and triangle waves.

The following example illustrates how the function generator loop operates. See figure 5-3. First, assume the comparator's output is high. This biases diode gate CR35 - CR38 to allow the current +COMP to flow into the resistor (R102) establishing the positive reference square wave voltage. The positive reference voltage is about +1.25V (V=+ICOMP x R102). Also, when the comparator output is high, the diode gate (CR27 - CR30) is biased to allow the current, ISWITCH+, to charge the Frequency Range Capacitor. Charging the capacitor with a constant current produces a linear ramp. The Triangle Buffer isolates the Frequency Range Capacitor from the Comparator. When the ramp voltage reaches the positive reference square voltage, the Comparator output switches low. When the comparator's output is low, diode gate (CR35 - CR38) switches and allows the current -COMP to flow from resistor (R102) establishing the negative reference square wave voltage - about –1.25V. At the same time, the comparator switches diode gate (CR27 - CR30) and allows the current ISWITCH– to discharge the Frequency Range Capacitor. This cycle repeats producing simultaneous triangle and square waves. The timing diagram with figure 5-3 illustrates waveform timing.

The VCG Summing Amplifier and Symmetry control the magnitude of the currents ISWITCH+ and ISWTCH-. The Frequency Range Capacitor determines

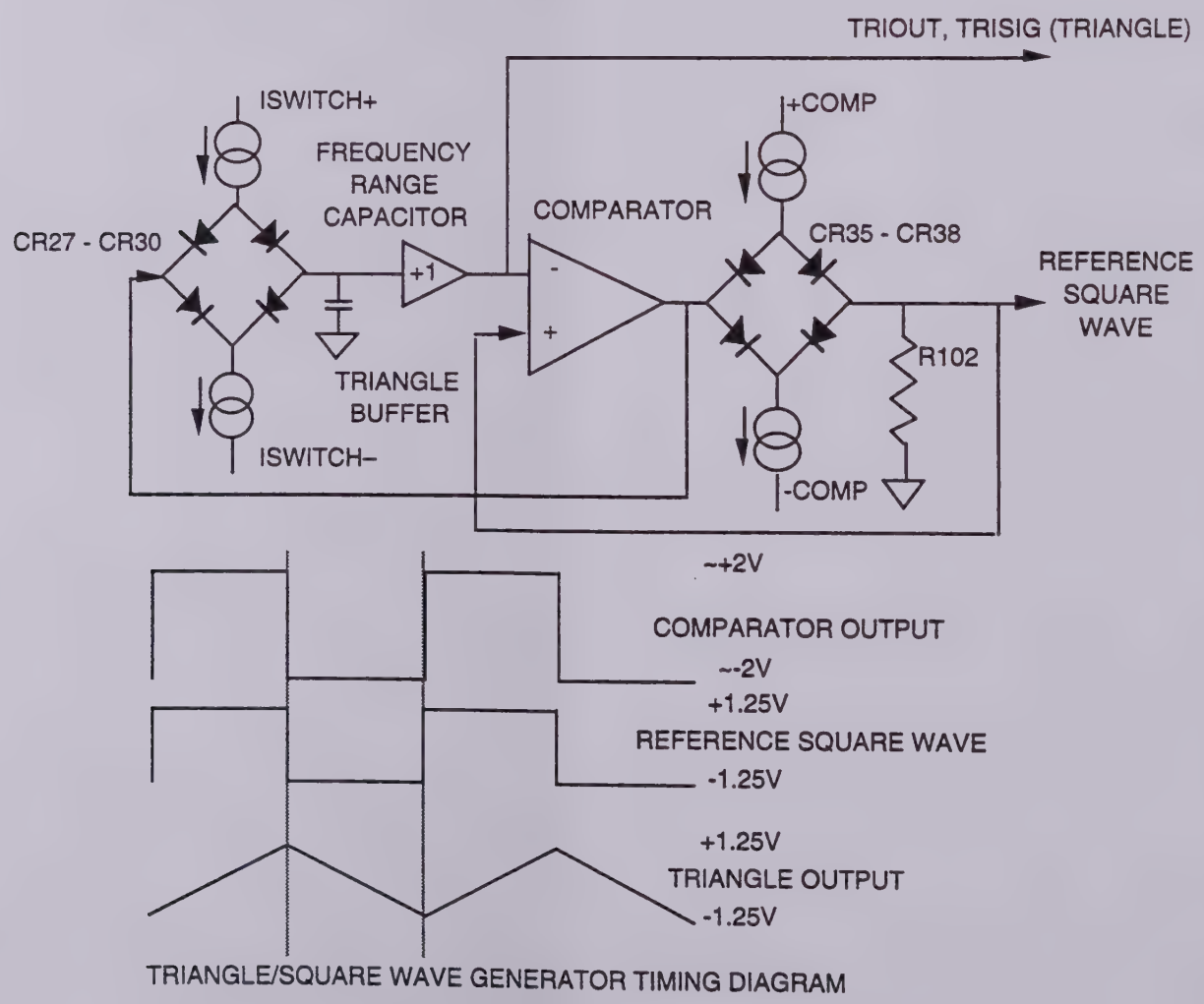



**Figure 5-3. Function Generator Loop**

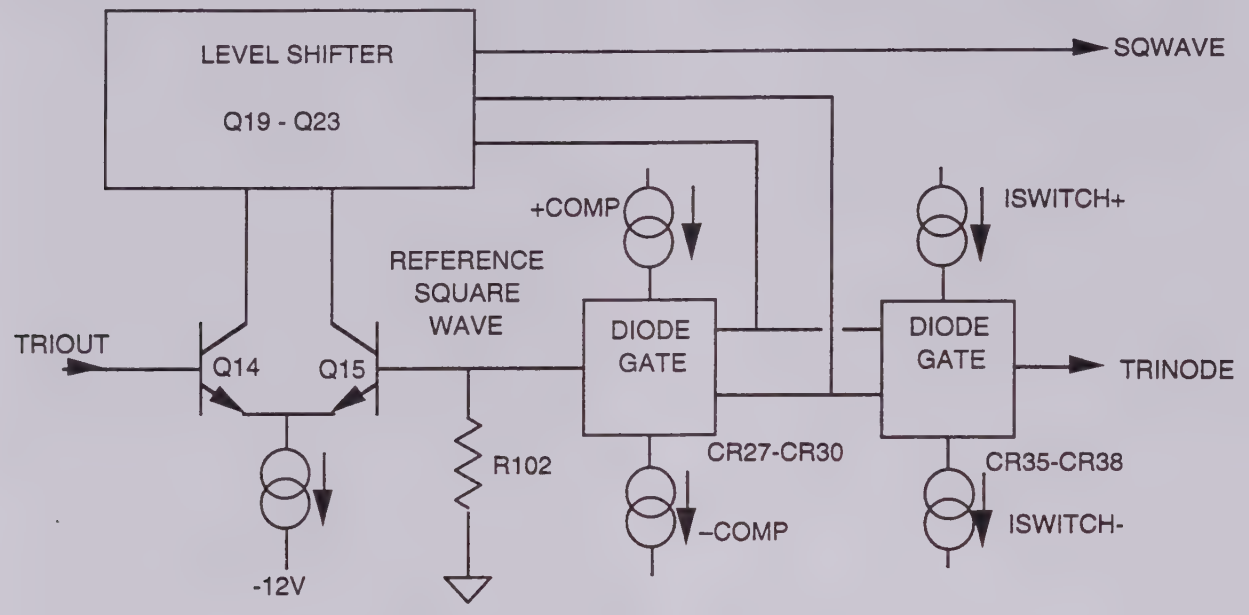



**Figure 5-4. Simplified Comparator**

the waveform's frequency range. Increasing the currents increases the frequency. Increasing the Frequency Range Capacitor decreases the frequency. The opposite of each is also true.

Normally, the current sources, ISWITCH+ and ISWITCH–, produce equal but opposite polarity currents. To change the symmetry (duty cycle) of the waveform, the Model 90 changes the ratio of the current sources. For example, the ISWITCH+ source may supply more than half of the current, while the ISWITCH– source may supply less than half of the current.

### 5.2.2.1 Comparator

The Comparator (schematic 1104-00-3342 sheet 7 of 7) compares the output from the triangle buffer, TRIOUT, to the reference square wave level and produces an output that drives both diode gates. Figure 5-4 provides a simplified comparator circuit.

The transistors (Q14 and Q15), connected as a differential amplifier, compare the TRIOUT (base Q14) to the reference square wave. The level shifter (Q19, Q20, Q21, Q22 and Q23) converts the input from Q14 and Q15 collector signals into a bipolar signal that can drive the diode gates and the SQWAVE output. Diode gate (CR27, CR28, CR29, CR30) switches between the compensation current sources (+COMP and –COMP) to generate the reference square wave (ICOMP x R102).

The compensation current source is adjustable over a small range in order to provide high-frequency compensation (paragraph 5.2.5). The comparator also drives the other diode gate (CR35, CR36, CR37, CR38) which switches the VCG current sources (ISWITCH+ and ISWITCH–). These currents charge and discharge the Frequency Range Capacitor. Two JFETs (Q25 and Q26) buffer the diode gate (CR27 - CR30) from the ISWITCH+ and ISWITCH– current sources.

### 5.2.2.2 VCG Current Sources

The VCG current sources (schematic 1104-00-3342 sheet 3 of 7) convert the two symmetry control voltages, +FCV and –FCV, into two currents ISWITCH + and ISWITCH –. Because the current sources are mirror images, only the positive current source will be described.

The positive current sources consist of two amplifiers (U13 and U14) and two transistors (Q1 and Q2). U13 and Q1 form a voltage to current converter. U13 forces the voltage drop across R31 to produce the current, $I_{R31}$. The current $I_{R31}$ also flows through the resistor R30 producing a voltage equal to +FCV. The current mirror stage (U14 and Q2) forces a voltage drop across R36 equal to +FCV. The current through R36 is ISWITCH+ and drives the diode switch (CR35 - CR38). Another output from this current source, VSOURCE, drives the Trigger Baseline Compensation circuit.

The negative current source (U17, Q3, U18, Q4) is identical to the positive current source. U17 and Q3 form the voltage to current converter, and U18 and Q4 forms the current mirror.

During symmetrical operation (50%) the two resistors (R31 and R32) connect directly to ground. But selecting variable symmetry places R131 between the junction of R31 and R32 and ground. The control line $\overline{\text{SYM ON}}$ switches R131.

### 5.2.2.3 Frequency Range Capacitors

The frequency range switches (schematic 1104-00-3342 sheet 5 of 7) change the four frequency range capacitors to the TRINODE line. On the 20 MHz range, the timing capacitance is made up of a 15 pF capacitor (C67) and stray capacitance about 50 pF total; all other capacitors are switched out. For the 2 MHz through 200 Hz ranges, capacitance is added by relay or transistor switches, table 5-1 lists the capacitance for each range. Below 200 Hz, the capacitance multiplier controls the "capacitance".

When the continuous, AM, or SCM mode is selected, the Model 90 uses only the top decade of each frequency range which allows a 10:1 frequency change. But when the FM/VCG or Sweep mode is selected, the Model 90 locks the range switching to the frequency range of the programmed upper frequency and allows the frequency to be changed a full three decades or 1000:1 frequency change. Table 5-1 lists the frequency range for both types of conditions.

Capacitance for the 2MHz, 200 kHz, 20 kHz, and 2kHz ranges is controlled by relay or transistor switches which are enabled by control lines from the boards interface logic. When a control line goes low, the capacitor is switched in. Table 5-1 lists the control lines and their associated ranges and capacitors. Paragraph 5.6.4.1 describes the function generator interface logic.

When non-symmetrical waveforms are selected, the Model 90 switches to the next higher range to compensate for a 1/10th decrease in current source output.

### 5.2.2.4 Capacitance Multiplier

Lower frequencies require larger capacitors that often fail to maintain the precise value over time needed for accurate frequencies. To eliminate the need for large capacitors, the Model 90 uses a Capacitance Multiplier (schematic 1104-00-3342 sheet 6 of 7) to simulate large capacitors by dividing the current at the TRINODE. When the VCG Current Source supplies current, ISWITCH+, to the Frequency Range Capacitor, the Capacitance Multiplier draws a portion of the current from TRINODE to decrease the charging time. When the VCG Current Source draws current, SWITCH–, from the Frequency Range Capacitor, the capacitance multiplier adds current to TRINODE to decrease the discharging time.

The capacitance multiplier consists of two amplifiers (U23 and U24). The amplifier (U23) acts as a non-inverting amplifier that generates an amplified version of the TRINODE triangle waveform on one side of C62. A capacitor converts a constant slope voltage into a constant current, thus the capacitor (C62) converts the triangle voltage into a current "square wave" at the inverting input of the amplifier (U24). The output of U24, TP11, contains a square wave which is 180° out of phase with the function generator's triangle (figure 5-3). The signal at TP11 is a composite of the out-of-phase square wave and the in phase triangle because the triangle connects directly to the non-inverting input of U24. The output from U24 drives the resistor (R129) with the composite signal. But since both sides of R129 have a triangle signal, the differential signal will be the square wave which causes constant current in R129 in alternating directions with the square wave. When the ISWITCH+ is selected by the diode bridge, most of the charging current is drawn out of the TRINODE through R129 to the negative portion of the square wave at TP11. When ISWITCH- is selected, the positive portion of the square wave sources current through R129 to TRINODE. The net effect is the frequency range capacitor is charged and discharged at a slower rate when the relay (K4) switches the Capacitance Multiplier to the TRINODE. Resistors R67, R68, R69, and R71 determine the square current to inverted square voltage gain of U24, and generate the bottom four frequency ranges of the function generator. Refer to table 5-2.

When the continuous, AM, or SCM mode is selected, the Model 90 uses only the top decade of each frequency range which allows a 10:1 frequency change. But when the FM/VCG or Sweep mode is selected, the Model 90 locks the range switching to the frequency range of the programmed upper frequency and allows the frequency to changed a full three decades or 1000:1 frequency change. Table 5-2 lists the frequency range for both types of conditions.

### 5.2.2.5 Triangle Buffer

The triangle buffer (schematic 1104-00-3342 sheet 6 of 7) isolates the triangle node, TRINODE, from the buffer's output, TRIOUT. The triangle buffer consists of a source follower (Q11) buffered by an emitter follower (Q12). The circuit provides dc stability by monitoring the input and outputs with U25 and controlling the drain

Table 5-1. Range Control and Values >200 Hz

| Frequency Range | | | |
|---|---|---|---|
| CW, AM, and SCM 10:1 - Top Decade | VCG/FM and Sweep 1000:1 Three Decades | Capacitance | Control Lines |
| 20 -2 MHz | 20 MHz - 20 kHz | 50 pF - (15 pF + Stray) C67 | None |
| 2MHz - 200 kHz | 2MHz - 2kHz | 490 pF - C57, C58, C67 | $\leq\overline{FR8}$ |
| 200 kHz - 20 kHz | 200 kHz - 200 Hz | 0.00519 µF - C55,C57, C58, C67 | $\leq\overline{FR7}$, $\leq\overline{FR8}$ |
| 20 kHz - 2kHz | 20 kHz - 20 Hz | 0.05219 µF - C53,C55,C57, C58, C67 | $\leq\overline{FR6}$, $\leq\overline{FR7}$, $\leq\overline{FR8}$ |
| 2kHz - 200 Hz | 2kHz - 2Hz | 0.52219 µF - C52, C53,C55,C57, C58, C67 | $\leq\overline{FR5}$, $\leq\overline{FR6}$, $\leq\overline{FR7}$ $\leq\overline{FR8}$ |

to source current in Q11 so $V_{CS}$ = 0V. Q13 is the controlled current source.

### 5.2.3 VCG Summing Amplifier

The VCG Summing Amplifier (U5 - schematic 1104-00-3342 sheet 2 of 7) algebraically adds the MOD IN, VFREQ, SWEEP, and VLOOP inputs. These input signals control the frequency of the function generator's waveform. MOD IN is the FM/VCG input which can be an ac or dc signal. VFREQ is a dc value representing the function generator's fixed frequency. The DAC Sample and Hold Network on the Motherboard (schematic 1104-00-3395 sheet 5 of 10) supplies the VFREQ signal. The Sweep Generator (schematic 1104-00-3342 sheet 2 of 7) produces a ramp that drives the SWEEP input. VLOOP is an analog frequency correction signal supplied by the phase lock loop. Another input, VCGZERO, is an Autocal correction voltage supplied by the DAC Sample and Hold Network on the Motherboard. Output from the VCG Summing amplifier, VSUM, drives the Symmetry Control (paragraph 5.2.4).

Most inputs to the VCG Summing Amplifier are connected by analog switches (U4A - U4D). Each switch is controlled by a control line from the board's interface logic. The MOD IN signal connects to the amplifier when $\overline{FM}$ line (U4A) goes low. At the same time, the FM line goes high disconnecting (U4D) the FM/VCG input resistor (R3) from ground. When FM/VCG is not selected, switch (U4D) is closed. Control line $\leq\overline{FR7}$ switches in added phase lock filtering at 200 kHz and below. When the frequency is set to <20 mHz (FR0) or symmetry is not 50%, the control line $\overline{SCALE}$ inserts a resistor (R8) which divides the VFREQ input by 10 allowing the unit to operate on the middle decade of the selected frequency range. All control lines used in the VCG Summing Amplifier are supplied from the Function Generator Input Logic (paragraph 5.6.4.1).

### 5.2.4 Symmetry Control

Symmetry Control (schematic 1104-00-3342 sheet 3 of 7) controls the symmetry of the function generator waveform. The input, VSUM, from the VCG Summing Amplifier drives two similar circuits, one controlling the charging time (U7C) and the other controlling the discharging time (U7D). The two outputs from the circuit (+FCV and -FCV) supply equal but opposite polarity (50% symmetry) voltages. These two voltages drive the VCG Current Sources, as well as, the High Frequency Compensation circuit.

The +FCV circuit consists of the inverting amplifier (U9) with the DAC (U7C, U10) that controls the gain of the circuit. The DAC (U12B, U11A) provides an offset adjustment. The Microprocessor Section on the Motherboard loads the data values into the DACs.

The –FCV circuit consists of the non-inverting amplifier (U15) with the DAC (U7D, U16) controlling the gain. The DAC (U12A, U11B) provides an offset adjustment. The Microprocessor Section on the Motherboard loads the data values into the DACs.

At 50% symmetry (symmetrical waveform), each circuit provides equal outputs. As the symmetry setting changes away from 50% in either direction, one circuit provides greater amplification and the other less amplification. The DACs by themselves provide linear gain, but placing them in the feedback paths of U9 and U14 provides an overall circuit gain of the inverse function of the symmetry setting.

The Autocal circuit measures the +FCV and –FCV voltage and provides correction values to the offset DACs data lines.

### 5.2.5 High Frequency Compensation

The High Frequency Compensation circuit (schematic 1104-00-3342 sheet 4 of 7) corrects for Internal circuit time delays of the function generator loop on the 200

Table 5-2. Range Control and Values <200 Hz

| Frequency Range | | | |
|---|---|---|---|
| CW, AM, and SCM | VCG/FM and Sweep | | |
| 10:1 - Top Decade | 1000:1 Three Decades | Resistance | Control Lines |
| 200 Hz - 20 Hz | 200 Hz - | 10 kΩ - R67 | $\overline{FR4}$ |
| 20 Hz - 2Hz | 20 Hz - 20 mHz | 110 kΩ - R67, R68 | $\overline{FR4}$, $\overline{FR3}$ |
| 2Hz - 200 mHz | 2Hz - 2mHz | 1.11 MΩ - R67, R68, R69 | $\overline{FR4}$, $\overline{FR3}$, $\overline{FR2}$ |
| 200 mHz - 20 mHz | 200 mHz - 2mHz | 11.11 MΩ - R67, R68, R69, R71 | All high |
| 20 mHz - 2mHz | 20 mHz - 2mHz | See Note | See Note |

Note:

The Model 90 does not switch to the 20 mHz range. It actually keeps the same range capacitors as the 200 mHz range, but it decreases the input to the VCG Summing Amplifier by 1/10th effectively dropping down a decade range by switching in, $\overline{SCALE}$,an additional input resistor (R8) in series with the VFREQ input.

kHz to 2 MHz and 2 MHz to 20 MHz frequency ranges by decreasing the current, +COMP and –COMP, which decreases the reference square wave voltages. This causes the Comparator to switch sooner, cancelling the tendency of the triangle to grow in frequency as the frequency increases.

The High Frequency Compensation circuit consists of two DACs (U12C, U12D). The DAC uses the +FCV and –FCV voltage as reference voltages. The microprocessor section provides the DACs with data which adjusts the gain of the output. Outputs from the DACs (+COMP and –COMP) will be scaled from the +FCV and –FCV.

### Trigger Baseline Compensation

Trigger Baseline Compensation (schematic 1104-00-3342 sheet 4 of 7) controls the quiescent baseline level during non-continuous modes of operation. A single line, RUN, from Mode control (paragraph 5.5) controls the generation of the triangle wave by either forcing the TRINODE line to "ground" (trigger, gate, and burst modes) or "open" (continuous mode). With the RUN line low, the TRINODE line is forced to ground; with RUN high, the system operates in the normal manner.

The Trigger Baseline Compensation circuit consists of amplifiers (U19 and U20) and transistors (Q5, Q6, and Q7). Amplifier (U19) and transistor (Q5) form a voltage to current converter. A voltage equal to VSOURCE appears across the resistor (R38) producing a current $I_{R30}$. The current mirror (U20, Q7) reflects the current $I_{R30}$ off the –VCG supply. The drop across R39 also equals +FCV. U20 forces a drop equal to +FCV across R40, but R40 is half the value of R39 which produces a current equal to 2(ISWITCH+). When RUN goes high, the current, 2(ISWITCH+), flows through the diode (CR10) reverse biasing diodes CR7 and CR8. This releases the TRINODE line and allows the function generator to run.

When the RUN line goes low, the diode (CR10) is reversed biased and the current flows through diodes CR8 and CR9. A current equal to ISWITCH+ flows through each diode. This forces the TRINODE to ground potential and stops the function generator. The Mode Control and Bust Counter logic on the Arb Board controls the RUN line.

## 5.3 Output Section

### 5.3.1 General

The Model 90 output section (see figure 5-5) consists of nine circuit blocks: the Function Selector with Square Shaper, XY Multiplier, AM Summing Amplifier, Preamplifier, Power Amplifier, 0/20 dB Attenuator, Balanced Output Drivers, Unbalanced Output Attenuator Network and Impedance Control, and Balanced Output Attenuator network and Impedance Control. The output section, shown in figure 5-5, is located on three separate assemblies in the Model 90: Phase Lock Loop board, Output board and Motherboard. In figure 5-5, the bold lines represent the signal flow through the Output section. The waveform, selected by the Function Selector, flows through the XY Multiplier where its amplitude is determined by the amplitude controlling signal. The waveform is then amplified and routed through attenuators to the selected output connector. An optional High Voltage Output supplies another source of all functions but over an amplitude range of 1mVpp to 40 Vpp.

### 5.3.2 Square Shaper and Function Selector

The square shaper (schematic 1104-00-3335 sheet 2 of 5) converts the TTL level square wave signal (SQWAVE) from the Function Generator section to a bipolar, 2Vpp square wave. The shaper's input is a non-saturating input transistor (Q1), which produces fast switching edges. This transistor drives the level shifter (Q5 and Q6) whose output is a 3Vpp square wave which switches the diode gate (CR3 - CR6). The gate switches the positive and negative current sources which drive the load resistor (R16T). The +2 amplifier (U11) buffers the square wave and drives the Function Selector. The square wave level is approximately 1Vpp at TP1. The two transistors Q2 and Q4 are used to enable and disable the Square Shaper. When the SQRON line goes high, the Square Shaper is enabled.

The function selector circuit selects and routes either the Sine (SIN1), Triangle (TRIOUT), square (2Vpp SQUARE), or Arb (OPTSIG) waveform to the preamplifier (PREAMPIN). The function selector, located on the Output board, consists of four relays (K1 - triangle, K2 - square, K3 - sine, and K4 - Arb (schematic 1104-00-3335 sheet 2 of 6)). Microprocessor Section (schematic 1104-00-3395 sheet 3 of 10) switches the relays via the interface latch (U2 - schematic 0104-00-3335 sheet 1 of 6). When one of the relay control lines ($\overline{\text{SINSEL}}$, $\overline{\text{TRISEL}}$, $\overline{\text{SQSEL}}$, $\overline{\text{OPSEL}}$) goes low, the relay will be closed. Only one relay will close at a time. In addition, the function selector terminates each waveform input and sets the amplitude of each waveform to approximately 1Vpp using resistor networks.

### 5.3.3 XY Multiplier and Preamplifier

The XY Multiplier and Preamplifier (schematic 1104-00-3335 sheet 3 of 5) controls or modulates the amplitude of the selected function. The multiplier's Y input receives it's input (PREAMPIN) from the function selector. All function levels are about 1Vpp. The AM Summing Amplifier on the Phase Locked Loop board (schematic 1104-00-3341 sheet 6 of 6) supplies the multiplier's X input (AMSIG). A dc level at the X input controls the generator's amplitude level, and an ac signal modulates the generator's amplitude. The ±6V Supplies (U14A, U14D, Q27, and Q26) provides the power for the XY Multiplier.

The multiplier (U4) is a wide-band device producing differential output currents which are the product of the PREAMPIN signal and the AMSIG input. The resistors (R33 and R34) convert the multiplier's output current into voltage. A pair of Darlington emitter followers (Q22, Q23, Q24, and Q25) buffer the signal from the XY Multiplier's output and drives the differential amplifier (U5). The differential amplifier (U5) converts the differential output from the emitter followers to a single-ended output (PREOUT) of about 6Vpp (full amplitude). PREOUT is offset about +3.5 Vdc to compensate for offsets in the multiplier circuit. The multiplier offset circuit (U14C and U12) supplies a compensation voltage (COMPOUT) to the output amplifier which compensates for offset in the PREOUT signal.

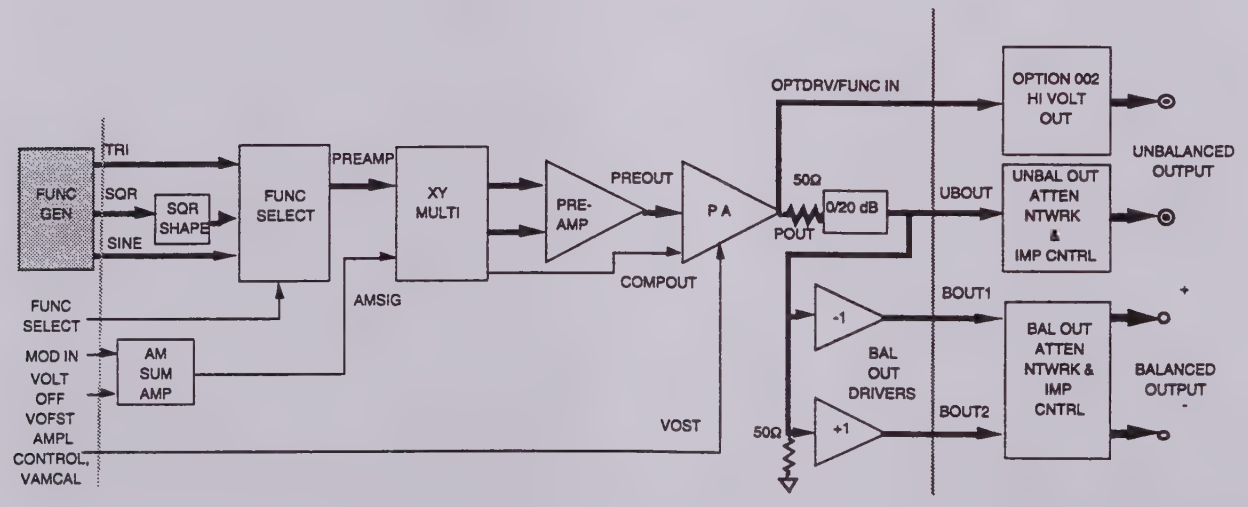



Figure 5-5. Output Section Block Diagram

### 5.3.4 Output Amplifier

The power amplifier (schematic 1104-00-3335 sheet 4 of 6) is a fixed gain, wide-band inverting amplifier with a push-pull complimentary symmetry output stage. This amplifier provides the gain and drive needed to drive the unit's outputs. The Output Amplifier has three signal inputs: PREOUT, COMPOUT, and VOFST. PREOUT is the selected function from the Preamplifier. COMPOUT is the multiplier compensating voltage from the multiplier's offset circuit. VOFST supplies the offset voltage to either dc offset the waveform or dc output level. VOFST is generated by the DAC Sample and Hold Network on the Motherboard. Both the COMPOUT and VOFST inputs contain inductors which improve the transient response.

The Output Amplifier has two distinct signal paths: the ac path and the dc path. The ac path provides the wide-band and high speed required by the unit's output (schematic 1104-00-3335 sheet 4 of 6). The ac path routes the signal through C36, C49, and the emitter followers Q12 and Q16 to the current sources Q13 and Q17. The emitter followers Q14, Q15, Q18, and Q19 buffer the current source from the PAOUT and feedback resistor R79 and R80. The dc path provides the low frequency path and dc stability of the output amplifier. The dc path runs through the differential amplifier Q9 and Q10. DC gain rolls off with frequency (about 80 kHz). The RC network C31 and R47 determines the roll-off frequency. The differential amplifier (Q9 and Q10) drives the inverting stage of Q11 whose output adjusts the dc bias of the current source. The amplifier's 50Ω output impedance is set by the resistors R95, R96, and R97. PAOUT also drives the Output Board's Peak Detector.

### 5.3.5 –20 dB Attenuator

The –20 dB attenuator circuit (schematic 1104-00-3335 sheet 5 of 6) together with the XY Multiplier and -40 dB Attenuators (Motherboard) controls the level of the output waveform. The -20 dB attenuator attenuates the power amplifier's PA OUT signal by switching in or out resistors R98 through R108. The microprocessor circuit via the Output board's data register (U3) closes the relay (K5) when the $\overline{\text{ATTEN-20}}$ goes low. R169T and C105T improves the transient response of the attenuator.

### 5.3.6 Balanced Drivers

The relay (K6 - schematic 1104-00-3335 sheet 5 OF 6) selects either the Balanced or Unbalanced output and routes the signal from the –20 dB attenuator to either the Unbalanced Output Attenuator Network and Impedance Network or to the Balanced Drivers. If balanced output is selected, the signal is routed through two amplifiers which produces two 180° out of phase signals, BOUT1 and BOUT2. The amplifier (U6) is a unity gain inverting amplifier. The other amplifier (U7) is a unity gain, non-inverting amplifier. The 50Ω source and load (R104 - R108) reduce the input level by 1/2 which produces a net gain of ±1/2 in the two amplifiers. The two outputs, BOUT2 and BOUT1, are routed to the Balanced Output Attenuator Network and Impedance Control (Motherboard). Both signals also drive the Peak Detector.

The balanced/unbalanced relay (K6) is controlled by the BAL-UB line from the latch (U3). When the BAL-UB line goes low, the Unbalanced output is selected. When the line goes high, the Balanced output is selected.

### 5.3.7 Unbalanced Output Attenuator Network and Impedance Control

The Unbalanced Output Attenuator Network and Impedance Control block on the Motherboard (schematic 1104-00-3395 sheet 7 of 10) serves two functions. It selects the output impedance of the instrument and provides 0dB or -40 dB of attenuation.

If the unbalanced output is selected, the UBOUT signal from the Balanced Driver is routed through a -40 dB attenuator (K1 – R69 through 74). The relays (K2 and K3) and their associated resistors select the output impedance (50Ω, 75Ω, or 600Ω). The relay (K6) opens the output when the Unbalanced Output is turned off. The output from this block drives the Unbalanced Output connector.

The attenuator relay (K1) is switched when U30 pin 15 goes low. When K2 and K3 are disabled (U30 pins 14 and 13 high), the output impedance is 50Ω. When relay K2 is disabled (U30 pin 14 high) and relay (K3) is enabled (U30 - pin 13 low), the output impedance is 75Ω. When both K2 and K3 are enabled (U30 - pins 14 and 13 low), the output impedance is 600Ω.

### 5.3.8 Balanced Output Attenuator Network and Impedance Control

The Balanced Output Attenuator Network and Impedance Control block on the Motherboard (schematic 1104-00-3395 sheet 7 of 10) serves two functions. It selects the output impedance of the instrument and provides –40 dB of attenuation.

If the balanced output is selected, the BOUT 1 and BOUT2 signals from the Balanced Driver are routed .through the –40 dB attenuator (K4 along with resistors R80 through R89). The relay (K5 and its resistors) select the output impedance (135Ω and 600Ω). The out-

put from this block drives the front panel's Balanced Output connectors.

The attenuator relay (K4) is switched when U30-pin 19 goes low. When K5 is disabled (U30 - pin 12 high), the balanced output impedance is 135Ω. When K5 is enabled (U30 - pin 12 low), the output impedance is 600Ω.

The control line, $\overline{POE}$, from the Microprocessor resets the attenuators to -40 dB at power up or power down.

### 5.3.9 High Voltage Output - Option 002

The High Voltage Output, a Model 90 option, provides a signal between 1mVpp to 40 Vpp of all functions. The High Voltage block (figure 5-6) consists of the input buffer, high voltage amplifier, and attenuators. The block receives its input from the standard power amplifier's output, PAOUT, which is attenuated by one-third and routed to the input buffer. The buffered signal can be routed either directly to the high voltage amplifier's input or through the 20 dB attenuator to the input of the amplifier. The high voltage amplifier provides the final gain and drive necessary to drive devices connected to the High Voltage Output connector. The output from the amplifier runs through the output attenuator which provides either direct output, 40 dB attenuation, or 60 dB attenuation.

Figure 5-6 indicates the voltage levels for points throughout the block. Those levels shown, such as 10 Vpp to 1Vpp, represents direct or 0dB flow. Levels , such as 0.99 Vpp to 0.1 Vpp represents levels of signal flowing through the 20 dB Attenuator. Also, the bold line signifies main signal flow, while the gray line signifies attenuated signal flow

#### 5.3.9.1 High Voltage Output Option Input

The High Voltage Output option receives its input from standard Power Amp output, PA_OUT (schematic 1104-00-3335 sheet 4 of 6). The attenuator (R115, R116 - schematic 1104-00-3335 sheet 6 of 6) divides the PA_OUT signal by one-third and route the signal, now called OPTDRV to the High Voltage Output's Input buffer. The input signal to the input buffer is called FUNC_IN (schematic 1104-00-3386 sheet 3 of 4).

The Power Amp supplies to the FUNC_IN a signal whose level can be varied between 10 Vpp to 1Vpp of all functions and modes of the Model 90. This signal also can be offset.

#### 5.3.9.2 Input Buffer and 20 dB Attenuator

The input buffer (U13 - schematic 1104-00-3386 sheet 3 of 3) isolates the input signal, FUNC_IN, from the 20 dB Attenuator and High Voltage Amplifier. The buffer provides unity gain and 0Ω output impedance. It's output drives both the 20 dB Attenuator and, via the relay (K1), to the input to the High Voltage Amplifier.

The 20 dB Attenuator consists of a 10:1 voltage divider (R21, R22) and a buffer (U14). The relay (K1) selects the attenuator when High Voltage output level is between 3.99 Vpp and 0.4 Vpp. Table 5-3 defines K1 setting for High Voltage Output ranges.

#### 5.3.9.3 High Voltage Amplifier

The High Voltage Amplifier is a wide-band, dc coupled amplifier with an overall gain of approximately four. The amplifier (schematic 1104-00-3386 sheet 3 of 4) consists of the input operational amplifier (U15), current sense transistors (Q4 and Q5), and output emitter followers (Q6, Q7, Q10, and Q11).

The input to the amplifier (U15) causes its output to swing in the same direction. The current sense transistors sense the change in amplifier power supply currents and drive the output emitter followers. The voltage supplied by the emitter followers is fed back through the resistor (R27) with the ratio (8:1) of the voltage divider (R27 and R28) determining the input amplifier output voltage.

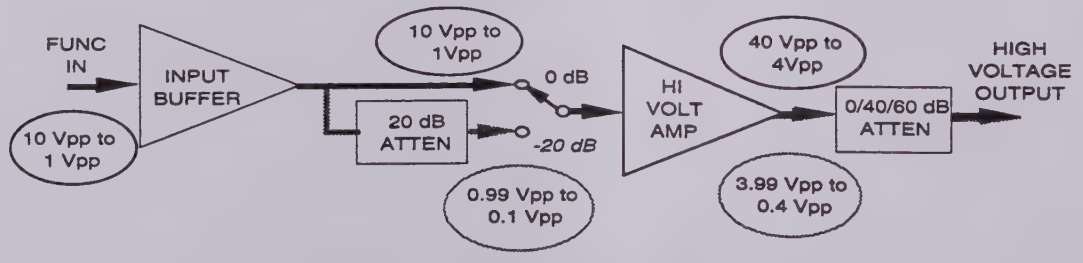



**Figure 5-6. High Voltage Output Option**

When the input swings positive, the amplifier output also swings positive. The amplifier draws more positive supply current (U15 pin 11) and less negative supply current (U15 pin 6). The positive current sense transistor (Q4) senses the increase in positive current and drives the parallel output emitter followers (Q6 and Q7) harder causing the output to swing positive. The negative current sense transistor (Q5) senses the decrease in current to the amplifier's negative supply and decreases the drive to the emitter followers (Q10 and Q11). When the input swings negative, the negative half increases, and the positive half decreases.

The low output voltage swing (<6V) of the input amplifier (U15) results in a wide bandwidth amplifier without slew rate limiting. The trim capacitor (C28) is used to adjust the amplifier's high speed peaking. The ratio (4:1) of the voltage divider (R25 and R26) determines the High Voltage amplifier's overall gain, -X4. Two transistors (Q8 and Q9) monitors the current supplied by one of each pair of output emitter follower, and if the High Voltage Output is short circuited, the transistors turn on and turn off the output emitter followers. Also, the output fuse (F1) protects the output emitter followers from external over voltages.

#### 5.3.9.4 0/40/60 dB Attenuator

The output signal from the High Voltage Amplifier runs the 0/40/60 dB Attenuator. The attenuator provides three levels of signal attenuation (0dB, 40 dB, and 60 dB), plus disconnecting the amplifier from the output connector. The attenuator consists of relays (K2, K3, and K4) which selects the attenuators and routes the signal to the High Voltage Output connector, and the attenuators (40 dB: R45 - R49; 60 dB: R50 - R53). The 0dB line contains the amplifier 5Ω source impedance resistor (R54 and R55). The relays are controlled by the three control lines that are supplied by the Aux Boards Control I/O logic (schematic 1104-00-3386 sheet 1 of 4) and routed through the inverter (U16). Table 5-4 defines the control lines/relays for High Voltage Output ranges.

## 5.4. Frequency Control

### 5.4.1 Introduction

Frequency Control covers those items that affect the frequency of the Model 90. These items include the primary frequency control - VFREQ, the sweep generator, the phase lock loop and synthesizer, and Mod In (FM/VCG).

### 5.4.2 VFREQ

The VFREQ line is the basic frequency control for the Model 90. The line originates at the Motherboard's DAC Sample and Hold Network (paragraph 5.6.5) and runs to the Function Generator's VCG Summing Amplifier (paragraph 5.2.3). The VFRQ is a dc voltage between +8 Vdc and +0.8 Vdc which represents the programmed frequency of the unit. VFREQ controls the frequency in the Continuous and AM modes. For FM, VFREQ sets the center frequency. For VCG, VFREQ sets the minimum frequency. For sweep mode, the VFREQ sets the start frequency.

### 5.4.3 Sweep Generator

The Sweep Generator (schematic 1104-00-3342 sheet 2 of 7) consists of an 8-bit DAC (U7A) and its buffer amplifier (U8) which produces the sweep voltage (0 to +8V) for the function generator. Another part of the sweep generator, DAC (U7B), supplies the sweep output ramp to the Sweep Out connector. VFREQ from the DAC Sample and Hold Network sets the Function Generator to the start frequency (paragraphs 5.6.5 and 5.2.3). Another dc voltage from the DAC Sample and Hold Network, VSLEN, provides the reference for the sweep DAC (U7A). To produce the sweep, the Microprocessor sends sweep DAC data (0000 0000 to 1111 1111 for sweep up and 1111 1111 to 0000 0000 for sweep down) representing the sweep voltage for the function generator. Sweep time determines microprocessor generated data rate. The Microprocessor's data also determines the sweep shape: linear sweep or logarithmic sweep. The sweep DAC is hardwired in the

**Table 5-3. 20 dB Attenuator**

| Voltage Output | $\overline{\text{20DBEN}}$ (U16 Pin 4) | K1 Selection |
|---|---|---|
| 40 Vpp to 4Vpp | Low | 0dB |
| 3.99 Vpp to 0.4 Vpp | High | 20 dB |
| 0.399 Vpp to 0.04 Vpp | Low | 0dB |
| 39.9 mVpp to 4mVpp | Low | 0dB |
| 3.999 mVpp to 1mVpp | High | 20 dB (see table 5-4) |
| Output Off. | High | 20 dB (see table 5-4) |

Table 5-4. Output Attenuator

| Voltage Output | $\overline{40DBEN}$ | $\overline{60DBEN}$ | $\overline{LOAMPL}$ | Relay/Attenuator |
|---|---|---|---|---|
| 40 Vpp to 4Vpp | Low | Low | High | K2 Enabled / 0dB |
| 3.99 Vpp to 0.4 Vpp | Low | Low | High | K2 Enabled (see table 5-3) |
| 0.399 Vpp to 0.04 Vpp | High | Low | Low | K3 Enabled / 40 dB |
| 39.9 mVpp to 4mVpp | Low | High | Low | K4 Enabled / 60 dB |
| 3.999 mVpp to 1mVpp | Low | High | Low | K4 Enabled / 60 dB (see table 5-3) |
| Output Off. | Low | Low | Low | All relays de-energized (see table 5-3) |

write mode. The sweep DAC receives data input when the $A/\overline{B}$ and $\overline{DS2}$ lines are high, and the $\overline{DS1}$ line is low.

The DAC (U7B), part of the Sweep Generator DAC, and amplifier (U6B) supplies the SWEEP OUT ramp. The Microprocessor writes data (0000 0000 to 1111 1111 for sweep up or 1111 1111 to 0000 0000 for sweep down) to the DAC when the $\overline{DS1}$ and $A/\overline{B}$ lines are low, and $\overline{DS2}$ line is high. The shape of the output will always be linear regardless of whether linear or log sweep is selected. The sweep time determines the rate of the data from the Microprocessor. The DAC reference voltage, supplied by Zener diode (CR1) is –6 Vdc.

### 5.4.4 Phase Lock Loop/Synthesizer

#### 5.4.4.1 Introduction

Figure 5- 7 provides a simplified illustration of the Phase Lock Loop and Synthesizer. This circuit controls the frequency of the function generator when the Model 90 operates as a synthesizer or variable phase generator. The circuit consists of six blocks located on several assemblies. The Frequency Synthesizer supplies the accurate, stable 20 Hz to 20 MHz frequency reference for the Phase Detector when internal lock is selected. For external lock, the Phase Detector receives its reference via the TRIG/FREQ IN connector on the front panel.

The variable frequency input to the phase detector closes the loop back to the function generator. The frequency input selected depends on the function selected. Either the sine or triangle wave is routed through the Zero Crossing Detector producing a square wave output. The square wave frequency runs directly into the phase detector. The phase lock loop's output, VLOOP, provides one input to the function generator's VCG Summing Amplifier.

#### 5.4.4.2 Frequency Reference

There are two frequency references used in the phase lock loop: the internal frequency synthesizer and the external TRIG/FREQ IN. The internal frequency synthesizer produces a 20 Hz to 20 MHz TTL level output, SYNTH. The frequency synthesizer circuit (figure 5-8) consists of a 500 kHz reference, reference divider, phase detector, low pass filter, voltage controlled oscillator, +N divider, and +M divider. The frequency synthesizer circuit is located on the Motherboard (schematic 1104-0-3395 sheet 4 of 10).

#### 5.4.4.3 Sine/Tri Z-Crossing Detector

The Sine/Triangle Zero Crossing Detector (schematic 1104-00-3341 sheet 2 of 6) converts the sine wave or triangle signal, ZCSIG into a square wave. As the signal passes through its zero crossing point, the crossing detector dc output level changes high or low producing a square wave. This output is one of the input signals, Z-CROSS, to the source selector circuit. The zero crossing detector consists of a high speed comparator. Its feedback resistors (R2 and R3) ensure noise immunity. Two control lines, SELA and SELB, enable the Zero Crossing Detector.

#### 5.4.4.4 Source Selector

The source selector circuit (schematic 1104-00-3341 sheet 2 of 6) selects one of each set of frequency sources as inputs for the phase detector.

Reference Frequency Sources
- SYNTH - internal frequency synthesizer
- BXFREQ - external reference source (TRIG/LOCK IN connector)

Variable Frequency Sources
- SQWAVE - square wave
- PLS/SQR - Not used
- Z-CROSS - sine or triangle wave converted to square wave

Two control lines, SELA and SELB, to the Source Selector choose the frequency sources. One reference frequency source and one variable frequency source will be selected. When SYNTH is selected, SQWAVE will also be selected. When BXFREQ is selected, either of the three variable frequency waveforms can be selected. The $\overline{LOCK}$ line enables (low) the Source Selector.

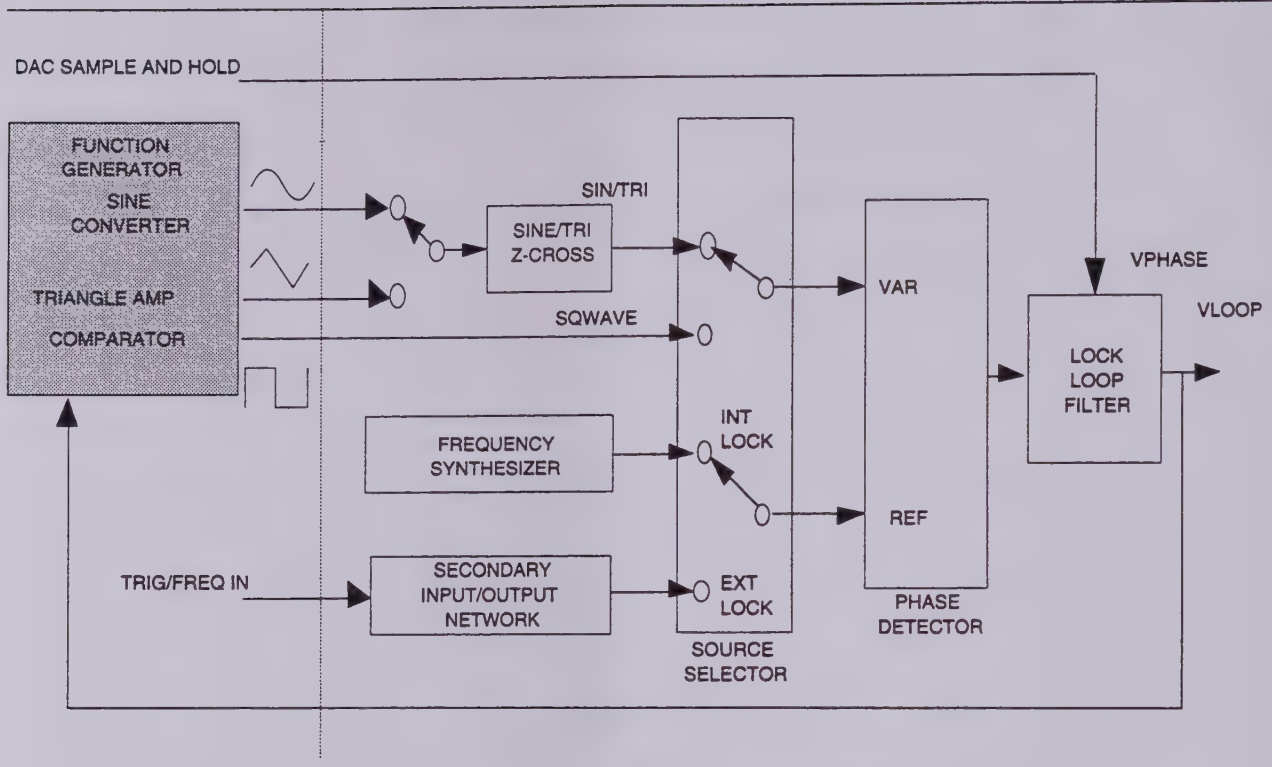



**Figure 5-7. Phase Lock Loop/Synthesizer**

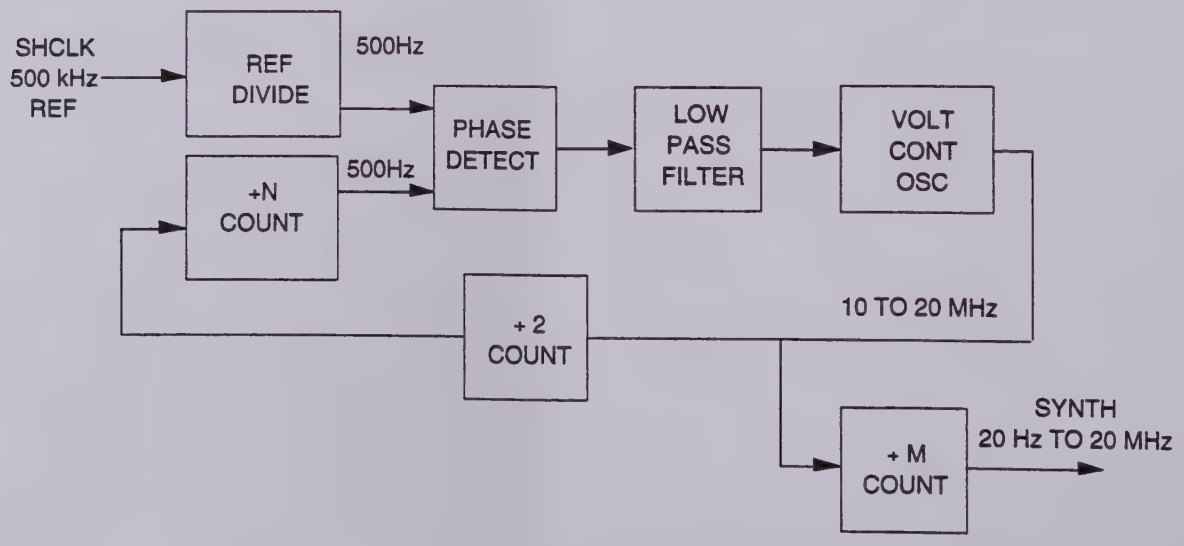



**Figure 5-8. Frequency Synthesizer**

### 5.4.4.5 Phase Detector

The Phase Detector consists of two biquinary (+2 and +5) Counters, the Phase Comparator, and the Charge Pump (schematic 1104-00-3341 sheets 2 and 3 of 6). Each input to the Phase Comparator runs through the +10 (20 - 2MHz range) or the +2 (all other ranges) counters (U4A and U4B) prescaling the input frequency. The phase comparator, a PAL, compares the reference frequency signal and the variable frequency signal, and produces an output based on edge arrival times of each monitored signal. The comparator generates one of three possible output conditions using the VLAGR and VLEADR lines. These lines drive the charge pump.

The Charge Pump (schematic 1104-00-3341 sheet 3) controls the current to and from the Lock Loop Filter. The Charge Pump consists of a diode gate (CR2 - CR5), a positive current source (Q1), and a negative current source (Q2). The diodes (CR1 and CR6) provide temperature compensation for their respective current sources. The VLAGR and VLEADR inputs from the phase comparator switch the charge pump current. The duration and direction of current represents the phase difference between the selected reference frequency signal and the variable frequency signal. The time difference between the edges determines the amount of current pumped into the lock loop filter. The phase difference between the edges determines the direction of current flow. When the signals arrive concurrently, no current is pumped to the Lock Loop Filter.

### 5.4.4.6 Lock Loop Filter

The Lock Loop Filter circuit (schematic 1104-00-3341 sheet 3 of 6) converts the pulsating current from the Charge Pump into a dc error voltage, VLOOP. The error voltage, VLOOP, gradually changes the VCG Summing Amplifier output signal, VSUM, to match the generator frequency and phase with the reference frequency.

When the reference to generator frequency difference is too large for the system to handle, the UNLOCK indicator on the front panel will flash. When FM or sweep modulation is selected, the $\overline{\text{LOCK}}$ line is high, opening the VLOOP line, and the UNLOCK indicator remains on.

The filter characteristics of the circuit are controlled by the Microprocessor Section, based on the signal frequency. Solid state switches (U17A - U17D) select the various filter circuit combinations. VPHASE supplies the voltage that varies the phase (PHASE key or PHASE command).

## 5.5 Mode Control

### 5.5.1 Introduction

Mode Control (schematic 1104-00-3327 sheet 2) turns on and off the Function Generator Loop (paragraph 5.2.2) via the control line, RUN. The Mode Control consists of the Mode Control GAL (U9), Burst Counter (U13), and Trigger Control (U12A), as well as the board I/O logic (schematic 1104-00-3327 sheet 2 of 8).

### 5.5.2 Mode Control

The Mode Control (U9) is a programmed GAL that serves several functions: function generator mode control and Arb clock control.

To control the function generator's operating mode, Mode Control decodes lines from the board I/O to control the Trigger Control (U12A). The input lines, MCNTL1 and MCNTL2 select the operating mode, and the input line, SRCNTL, selects the trigger source. SRCNTL low selects External Source, BXFEQ, and SRCNTL high selects Internal Source, SYNTH. Another line, MANTRIG, represents pressing the MAN TRIG key or its GPIB equivalent. The BURST line from the Burst Counter controls Mode Control in the burst and internal gate modes. Table 5-5 describes the relationship between the Mode Control input control lines and the selected modes. Mode Control produces three control lines; RSET, JSET, and KSET; for the trigger control.

### 5.5.3 Trigger Control

Trigger Control (U12A), a JK Flip Flop, provides the RUN line that controls the operation of the Function Generator (Trigger Baseline Compensation -paragraph 5.2.5).

Continuous Mode To place the function generator in the continuous mode, the Mode Control holds its RSET line low which forces the Trigger Control's RUN line high and allows the function generator to run.

Triggered Mode For the triggered mode, the Mode Control strobes the RSET line low to start the function generator after a triggering event. Also, the Mode Control holds JSET line low and KSET line high. The next negative transition of the SQR (square) from the function generator clocks the Trigger Control, which changes the RUN line to low and turns off the function generator. The function generator will always complete a full cycle.

Internal Gate and Burst Mode Internal gate mode is actually a burst mode. The Model 90 determines what

Table 5-5. Mode Control

| Control Line | Cont Mode | Trig Mode | Int Gate Mode | Ext Gate Mode | Burst Mode |
|---|---|---|---|---|---|
| MCNTL1 | 0 | 0 | 1 | 0 | 1 |
| MCNTL2 | 0 | 1 | 1 | 1 | 1 |

should be the correct number of cycles for 50% duty cycle of the internal gate frequency, and sets up the Burst Counter. The Mode Control strobes the RSET line low which starts the function generator. Also, the Mode Control places JSET high and KSET low. Once the Burst Counter determines the correct number of cycles has occurred, it places the Mode Control BURST high which sets JSET low and KSET high until the Trigger Control's QNOT line goes high.

External Gate The Mode Control strobes the RSET line low which starts the function generator. Also, the Mode Control holds JSET high and KSET low as long as the trigger input is true. When the trigger input goes false, JSET goes low and KSET goes high until the QNOT goes high.

### 5.5.4 Burst Counter

The Burst Counter (U13), a programmable +N down counter, signals the Mode Control when the programmed number of cycles is completed. The Microprocessor loads the serial data, BRSDIN, into the Burst Counter using the serial clock, BRCLK when the serial input is enabled, SRSEN. The counter, when clocked, BRCP, counts down to zero and the BURST line to the Mode Control goes low, indicating that the burst has been completed.

## 5.6 Microprocessor and Interfaces

### 5.6.1 Introduction

The Microprocessor and its interfaces provides the data processing and routing throughout the Model 90. This block includes the Microprocessor Section, Function Generator Interface, Arb Board Interface, Phase Lock Board Interface, Output Board Interface, Front Panel (Keyboard and Display) Interface, and the GPIB Interface. All interfaces, except the GPIB interface, are located on individual boards. Also, the DAC Sample and Hold Network and Internal Calibration Network operate with the Microprocessor Section. Figure 5-9 illustrates the relationship between the Microprocessor Section and Interfaces, as well as lists the Interface's enabling lines and data busses.

### 5.6.2 Microprocessor Section

The Microprocessor Section (schematic 1104-00-3395 sheet 3 of 10) controls all operations within the Model 90. The Microprocessor Section consists of the Microprocessor, Read Only Memory - ROM, Calibration/ Scratch Pad Memory, and Processor Support Chip, plus support circuits. The Microprocessor section receives its input data from the front panel or GPIB interface, processes the data, and provides data and control lines for internal operation. Figure 5-10 provides a simplified look at the Microprocessor Section.

The microprocessor (U6) executes operating instructions based on firmware stored in the ROM (U12). Another memory, the Calibration/Scratch Pad Memory (U11) - a Random Access Memory - RAM, stores the calibration data taken during Autocal and manual calibration. This memory also stores the instrument setup at power off and ten stored settings, as well as,

providing a temporary storage register during data processing. The RAM accepts data (writes) when its WE line goes low. If the WE line is high, the microprocessor section reads data from the RAM. A RAM backup battery (BT1) prevents the loss of data when power is turned off. A flashing life light verifies microprocessor sequencing. The PAL (U35) provides additional address decoding for the ROM (U12) expanding the memory size for the Model 90 firmware.

The Processor Support Chip (U7) controls the interfacing with other parts of the Model 90, as well as, decoding the lower eight address lines, A0 - A7. Seven card select lines from the Processor Support Chip enable interfaces in the Model 90.

| | |
|---|---|
| $\overline{\text{GPIB}}$ | GPIB interface |
| $\overline{\text{ROM}}$ | ROM via U35 |
| $\overline{\text{RAM}}$ | RAM via U35 |
| $\overline{\text{FPSTB}}$ | Front Panel |
| $\overline{\text{OBSTB}}$ | Output Board |
| $\overline{\text{FGSTB}}$ | Function Generator |
| $\overline{\text{OXSTB}}$ | Aux Board |

Four Quiet Address Lines, QA0 - QA3, address the board interfaces in the Model 90. In addition, the Processor Support Chip connects the eight Quiet Data Lines, QD0 - QD7, to the board interfaces in the Model 90. These lines are bidirectional and active when the

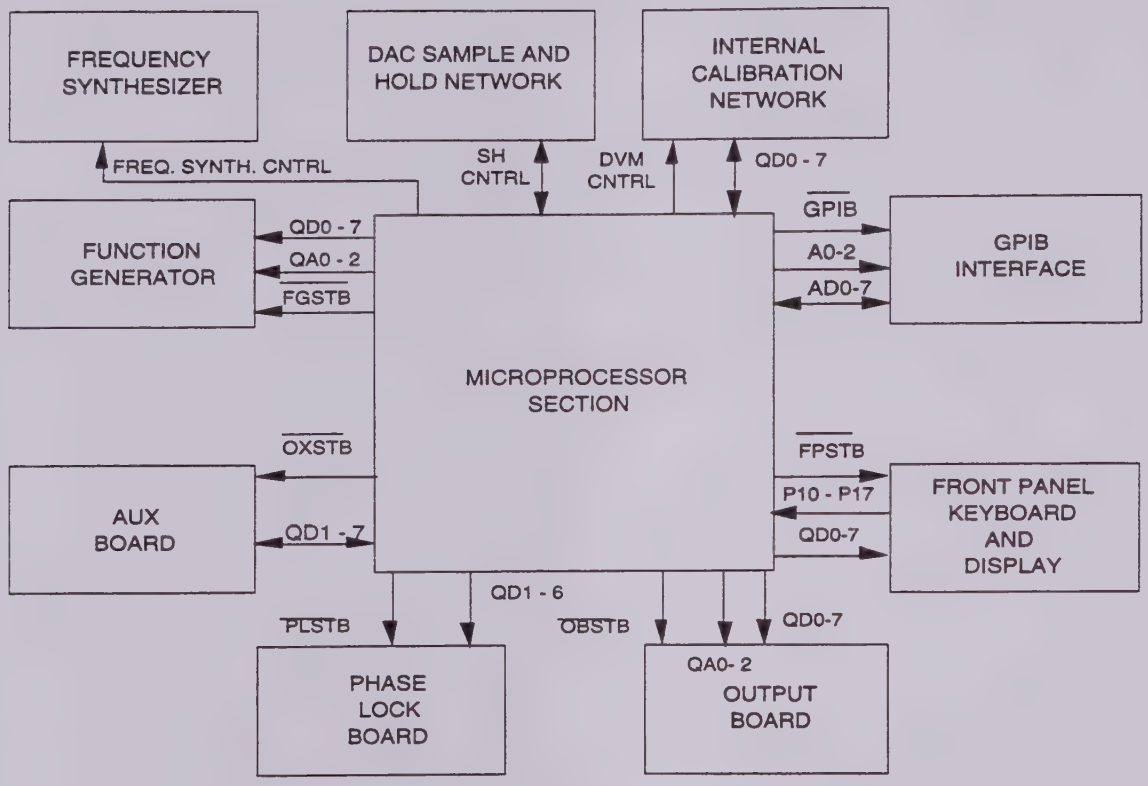



**Figure 5-9. Microprocessor and Interfaces**

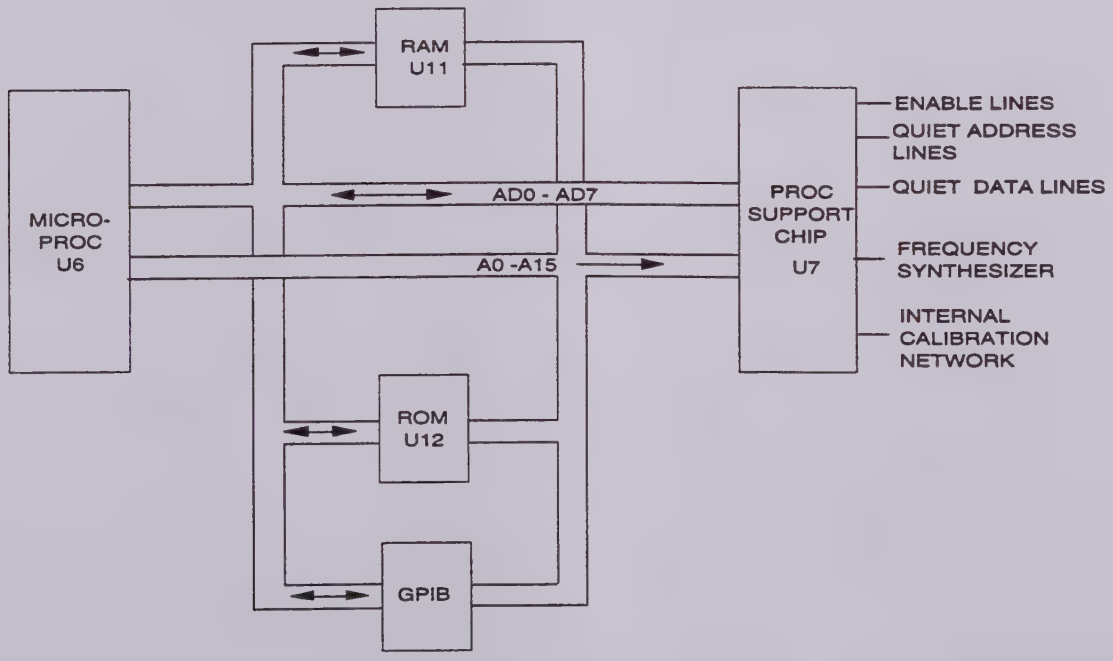



**Figure 5-10. Microprocessor Section**

microprocessor needs to communicate with the board interfaces.

Also, the Processor Support Chip controls the frequency synthesizer via the SEN, SDATA, and SCLK lines. SEN enables the synthesizer, SDATA supplies serial data which loads the synthesizer's +M and + N counters. SCLK clocks the data into the counters.

The Processor Support Chip also produces five sets of control lines for the Sample and Hold Network. The SHEN line enables the network's DAC. SHDATA supplies the serial data that loads the DAC, and SHCLK clocks the data into the DAC. SHSEQM enables the sample and hold selector channel. Three lines; SHSEL0, SHSEL 1, and SHSEL 2; select the sample and hold selector channels.

Another set of lines control the voltage measurement portion of the Model 90 internal calibration network. The lines, DVM0 - DVM5, select the inputs to the internal calibration network. $\overline{\text{DVMLB}}$ and $\overline{\text{DVMHB}}$ selects either the higher or lower order byte to be read by the microprocessor. DVMRUN instructs the DVM to run. DVM-RDY tells the microprocessor it has data to send. During the frequency related portion of the Autocal cycle, the Processor Support Chip and microprocessor measures the SQWAVE, BXFREQ, and SYNTH frequency, period and symmetry. The FREQOUT line connects the Processor Support Chip and the microprocessor.

Two lines, RKA and RKB, decode the rotary encoder's (front panel control knob) rotation.

### 5.6.3 GPIB Interface

The GPIB interface circuit (schematic 1104-00-3390 sheet 10) allows remote operation of the Model 90 using an external IEEE-488 compatible controller. All functions except power and GPIB address are programmable using the interface. The GPIB circuit consists of a GPIB controller and two transceivers.

The GPIB controller (U8) functions as a traffic controller, permitting data to flow in either direction when the correct control information is received. The 'handshaking' routine will ensure neither the signal generator nor the remote controller will send data faster than the other can use. The controller has internal registers where control, data, and address words are loaded and stored until needed or requested. The controller bus connects to the microprocessor circuit address bus A0 - A2. The identification address of an instrument is determined by five bits in the controller address register. The default address (09) automatically loads into the controller from RAM at first (cold start) turn-on. A new address can be entered using the front panel keyboard. The GPIB line from the processor support chip enables the GPIB interface. The E clock from the microprocessor supplies the timing for the GPIB controller. The $R/\overline{W}$ line (read - high, write - low) controls the direction of data flow through the GPIB controller.

The transceivers (U9 and U10) permit bidirectional data flow. They have sufficient input sensitivity to minimize false signals and sufficient drive current to minimize signal loss. The transceiver (U9) handles the GPIB data lines, and the transceiver (U10) handles the GPIB control lines. Direction of data flow through the transceivers is controlled by the GPIB interface chip's T/R2 line.

### 5.6.4 Board Interfaces

The following boards have interface logic circuits that converts data lines into control lines for use on that board.

Function Generator board-Schematic 1104-00-3342 1 of 7,
Phase Lock Loop Board-Schematic 1104-00-3341 1 of 6.
Aux Board-Schematic 1104-00-3386 1 of 8.
Output board-Schematic 1104-00-3335 1 of 6.
Display /keyboard of Front Panel-Schematic 0103-00-3001 3 of 3.

#### 5.6.4.1 Function Generator Interface

The function generator's interface logic consists of the input decoder (U1) and data registers (U2 and U3).

The decoder (U1) generates the clocks, CLK0 - CLK5, that will be used on the function generator board. The decoder inputs (QA0, QA1, and QA2) originate from the Microprocessor Section. The data clock selected by the address lines goes low at the decoder when $\overline{\text{FGSTB}}$ card select line goes low. Two enable lines of the decoder (G1 and G2A) are hardwired enabled. After the $\overline{\text{FGSTB}}$ card select line returns high, all decoder outputs return high. Table 5-6 provides a truth table for the decoder and defines the CLK outputs for the function generator board interface logic.

The registers (U2 and U3) latch data on their inputs on the rising edge of their clocks. The data is generated by the Microprocessor Section. The register (U3) supplies the frequency range control lines for the Frequency Range Switches and Capacitance Multiplier.

#### 5.6.4.2 Phase Lock Loop Interface

The phase lock loop board's interface logic consists of a single Octal data register (U1). The register latches the data on its input lines, QD0 - QD7, on the rising edge of

Table 5-6. Function Generator Decoder

| Decoder Inputs | | | | Output | Function |
|---|---|---|---|---|---|
| QA0 | QA1 | QA2 | $\overline{FGSTB}$ | | |
| 0 | 0 | 0 | ⊓ | CLK0 | Clocks Data Register U2 |
| 1 | 0 | 0 | ⊓ | CLK1 | Clocks $\overline{DS1}$ Sweep Generator |
| 0 | 1 | 0 | ⊓ | CLK2 | Clocks $\overline{DS2}$ Sweep Generator |
| 1 | 1 | 0 | ⊓ | CLK3 | Clocks $\overline{DS1}$ Symmetry Control |
| 0 | 0 | 1 | ⊓ | CLK4 | Clocks $\overline{DS2}$ Symmetry Control |
| 1 | 0 | 1 | ⊓ | CLK5 | Clocks Range Register U3 |
| 0 | 1 | 1 | ⊓ | $\overline{PLSTB}$ | Card select for Phase Lock Loop Interface |

the $\overline{PLSTB}$ card select line. The function generator interface supplies the card select line, and the Microprocessor Section supplies the data lines.

### 5.6.4.3 Aux Board Interface

The Aux board interface logic consists of an input decoder (U1), a data buffer (U2), and two octal data registers (U3 and U4).

The decoder (U1) selects the eight register clocks. Table 5-7 defines the decoder outputs. When a decoder is enabled (QA3 high) and $\overline{OXSTB}$ pulses low, a low pulse occurs on the decoder output line selected by QA0 - QA2. The data buffer (U2) isolates the quiet data lines, QD0 - QD7, from the registers. The registers latch data, AQD0 - AQD7, on the rising edge of their respective clocks.

### 5.6.4.4 Output Board Interface

The output board's interface logic consists of the input decoder (U1) and data registers (U2 and U3). The input decoder produces the clocks which drive the data registers. The decoder inputs originate from the Microprocessor Section. When the decoder is enabled and $\overline{OBSTB}$ pulse goes low, a low pulse occurs on the decoder output line selected by QA0 - QA2. The registers latch data, QD0 - QD7, on the rising edge of their respective clocks. Table 5-8 defines the decoder outputs.

### 5.6.4.5 Front Panel (Keyboard and Display)

The front panel provides local operator interface to the function generator. This assembly contains the following circuits:

Control Knob Circuit
Display
Keyboard Circuit
Annunciation Circuit

Control Knob The control knob (SW1 - schematic 1104-00-3001 sheet 1 of 3) rotates continuously in both directions. Control knob values per degree of turn depend on the function, mode, and range selected. Rotating the knob pulses its two output lines, RKA and RKB, with TTL logic levels. The Microprocessor Section on the motherboard counts these pulses to determine the amount of change and compares the phase relationship of the output lines to determine the direction of rotation.

Display The display (schematic 0103-00-3001 sheet 1 of 3) consists of the display driver (U1), Vacuum Fluorescent display (VFD1), and data latch (U3). The VFD is a triode vacuum tube with phosphorus coated anode that illuminates when electrons strike it. Each digit consists of 16 anodes with one grid. Elements of a digit lights when both the anode (+15V) and grid (+15V) are biased on. A -24V biases the grids off. The display driver (U1) controls the multiplexed arrangement of anodes and grids.

Table 5-7. Aux Decoder

| Decoder Inputs | | | | | Output | Function |
|---|---|---|---|---|---|---|
| QA0 | QA1 | QA2 | QA3 | $\overline{OXSTB}$ | | |
| 0 | 0 | 0 | 1 | ⊓ | $\overline{CLK0}$ | Clocks Data Register U3 |
| 1 | 0 | 0 | 1 | ⊓ | $\overline{CLK1}$ | Clocks Data Resister U4 |

The driver receives clocked, DSCLK, serial data, DSDATA, from the input latch (U3) via the level shifters (Q1 and Q2). Another line to the driver, DSPOR, provides a power on reset to the driver.

The display circuit is powered by its own +15 V dc regulator (VR1) which uses the +22 V dc for its input. The fluorescent display filament ($8V_{rms}$ superimposed on -15Vdc) receives its power from the FILA and FILB lines. All power is supplied from the motherboard.

Keyboard The keyboard circuit (schematic 0103-00-3001 sheet 1 of 3) consists of an eight-column, six-row matrix, input register (U3), and decoder (U2). Control signal, FPREG, latches the quiet data bus, QD0-QD2, lines into the latch which drives the decoder. The decoder steps through the six rows, making each row high (+5V) one at a time. When a key is pressed, the high appears on the column associated with that switch. The column lines (P10 - P17) connect directly to the microprocessor circuit. The microprocessor determines which key has been pressed by analyzing the row/column status.

Annunciator Circuit The Light Emitting Diode, LED, circuit (schematic 1104-00-3344 sheets 2 and 3) consists of LEDs (CR4 - CR27), decoder (U4), and data register (U5 - U7). The LEDs identify the selected mode and function. Two other LEDs (CR1 and CR2) connected to the data register (U3) are also part of the LED circuit. The decoder (U4) converts quiet addresses, QA0 and QA1, into clocks for the four registers. Each of four registers (U3, U5 - U7) reads the quiet data bus, QD0 - QD7, and when any of the latches goes low, the LED annunciator lights. Conversely, when a latch output goes high, the LED annunciator remains off.

### 5.8.5 DAC Sample and Hold Network

The DAC/Sample and Hold Network (schematic 1104-00-3395 sheet 5 of 10) provides the various control voltages required throughout the Model 90. The values for these control voltages are determined during Autocal and calibration. This circuit consists of the 16 bit DAC (U18), the 1 of 8 selector (U19), and the eight hold capacitors (C49 - 56) and buffers.

The microprocessor section loads serial data, SHDATA, using the clock, SHCLK. The line, SHEN, enables the DAC. Output from the DAC drives the selector. The microprocessor section's SHSEL0 - SHSEL2 lines select the channel. The voltage from the selector charges the selected capacitor (C49 - C56). The microprocessor section updates the DAC and selects the next channel. Thus, the microprocessor cycles through channels continuously refreshing the capacitors. Buffers (U20 - U24) provide a high impedance which hold the charge on the capacitors.

The DAC supplies a maximum output of ±3 Vdc. Some control voltages require voltages greater than the ±3 Vdc, therefore, some control voltages are amplified.

### 5.8.6 Internal Calibration Network

During Autocal, the Internal Calibration Network, in conjunction with circuits on other boards, makes various voltage and frequency measurements and stores correction data in memory. On power up, these correction values are recalled from memory and, via the Sample and Hold Network, routed to control circuits within the Model 90. Each of the test points may have more than one value; for example frequency related test points may have different values for different frequency ranges. Figure 5-11 illustrates the entire internal calibration network used with in the Model 90. The network shown can simply be thought of as a series of selector switches that ultimately route a single test point to the DVM. The calibration network consists of two parts: the voltage measurement section (schematic 1104-00-3395 sheet 2 of 10) and the frequency measurement section (schematic 1104-00-3395 sheet 3 of 10). Both sections provide inputs to the Microprocessor section, or to be more specific, the Processor Support Chip

The heart of the voltage measurement section is the DVM (U4 - Motherboard). The DVM receives a single dc voltage from the Multiplexer, Mux, (U3). The DVM is referenced to the +10 Vdc voltage reference (U32 - schematic 1104-00-3395 sheet 8 of 10).

The DVM MUX 1 (U3 - schematic 1104-00-3395 sheet 2 of 10) selects one of its eight inputs for the DVM.

**Table 5-8. Output Decoder**

| Decoder Inputs | | | | Output | Function |
|---|---|---|---|---|---|
| QA0 | QA1 | QA2 | $\overline{\text{OBSTB}}$ | | |
| 0 | 0 | 0 | ⊓ | CLK0 | Clocks Attenuator Selector (Motherboard) |
| 1 | 0 | 0 | ⊓ | CLK1 | Clocks Data Register U3 |
| 1 | 1 | 0 | ⊓ | CLK33 | Clock Data Register U2 |

Table 5-9 describes the control lines, inputs and the function of the Mux inputs. Test points connected to this multiplexer comes from either the Motherboard or other multiplexers.

The DVM MUX 2 (U1 - Schematic 1104-00-3395 sheet 2 of 10) also selects one of eight inputs. But, its inputs originate on the Output, Phase Lock Loop, and Function Generator boards. Table 5-10 describes the inputs and the control lines (DVM3, DVM4, and DVM5) that selects them. This mux provides two outputs. A direct output for voltages less than +4Vdc, and a reduced (1/2) output for voltages greater than +4Vdc.

The function generator's Autocalibration circuit (schematic 1104-00-3342 sheet 4 of 7) consists of an analog multiplexer (U28) which selects one of eight test points on the function generator board. The amplifier, U29A buffers the multiplexer's output. Another amplifier, U29B, amplifies the lower level signals by X101. The two amplifier outputs (FSTST and FGTST100) drives the Internal Calibration Network's DVM MUX 2. Table 5-11 describes the inputs and the control lines (A0, A1, and A2) that selects them.

The Output Board's Peak Detector (schematic 1104-00-3335 sheet 6 of 6) selects and routes one of four voltages to the positive and negative Peak Detectors. The Peak Detectors consist of a positive half (U9A and U9D) and a negative half (U9B and U9C). Both detectors function the same, except for the polarity of the outputs, therefore only the positive peak detector will be described. Applying a positive voltage to U9A causes the amplifier's output to swing positive charging capacitor (C69) through diode (CR28). The amplifier (U9D) buffers the capacitor's voltage and provides feedback to the input amplifier (U9A). As the input voltage is reduced, the diode (CR28) becomes reversed biased and the capacitor (C69) holds a charge that represents the most positive (peak) voltage. The diode (CR35) provides local feedback to the input amplifier (U9A) while holding the peak. The transistor (Q20) discharges the capacitor (C69) when the PKRST line

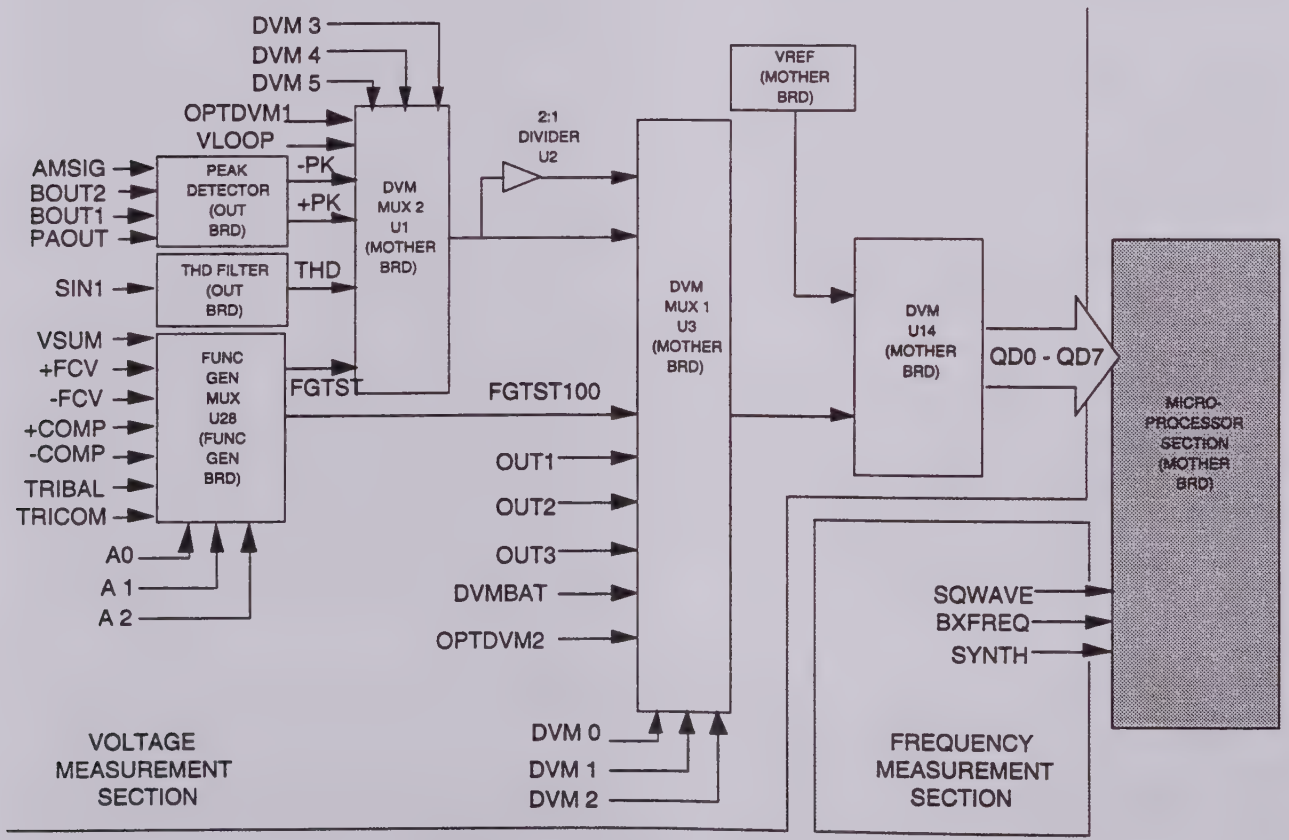



**Figure 5-11. Internal Calibration**

Table 5-9. DVM Mux 1

| DVM0 | DVM1 | DVM2 | Name | Function |
|---|---|---|---|---|
| 0 | 0 | 0 | OUT1 | Unbalanced output from Unbalanced Output and Impedance Network" |
| 1 | 0 | 0 | OUT2 | BAL OUT (+) from Balanced Output Attenuator Network and Impedance Control |
| 0 | 1 | 0 | OUT3 | BAL OUT (-) from Balanced Output Attenuator Network and Impedance Control |
| 1 | 1 | 0 | FGTST100 | Low level function generator measurements |
| 0 | 0 | 1 | DVM BAT | Measures memory back up battery voltage Microprocessor Section |
| 1 | 0 | 1 | OPTDVM2 | Identifies Option 001 / 002. |
| 0 | 1 | 1 | | Output from DVM MUX2. Voltages >+4V. |
| 1 | 1 | 1 | | Output from DVM MUX2. Voltages <+4V. |

Table 5-10. DVM Mux 2

| DVM3 | DVM4 | DVM5 | Name | Function |
|---|---|---|---|---|
| 0 | 0 | 0 | FGTST | Output from Function Generator Mux U28 on Function Generator Board. |
| 1 | 0 | 0 | TEST IN | TP 1 |
| 0 | 1 | 0 | +PK | Positive peak detector output from Output Board |
| 1 | 1 | 0 | THD | THD filter output from Output Board. |
| 0 | 0 | 1 | Ground | Circuit Common |
| 1 | 0 | 1 | -PK | Negative peak detector output from Output Board |
| 0 | 1 | 1 | VLOOP | Phase Lock Loop filter output from Phase Lock Loop Board |
| 1 | 1 | 1 | OPTDVM1 | Optional High Voltage Output amplifier output. |

Table 5-11. Function Generator Mux.

| A0 | A1 | A2 | Name | Function |
|---|---|---|---|---|
| 0 | 0 | 0 | Ground | Analog Ground |
| 1 | 0 | 0 | VSUM | VCG Summing Amplifier Output from Function Generator Board. |
| 0 | 1 | 0 | +FCV | Positive Symmetry Control output from Function Generator Board. |
| 1 | 1 | 0 | -FCV | Negative Symmetry Control output from Function Generator Board. |
| 0 | 0 | 1 | +COMP | Positive Output from the High Frequency Compensation DAC on the Function Generator Board |
| 1 | 0 | 1 | -COMP | Negative Output from the High Frequency Compensation DAC on the Function Generator Board. |
| 0 | 1 | 1 | TRIBAL | Triangle Buffer output from the Function Generator Board |
| 1 | 1 | 1 | TRICOM | Triangle Buffer's Analog Ground from the Function Generator Board |

Table 5-12. Peak Detector

| Control Line | Input Name | Function |
|---|---|---|
| $\overline{\text{SELPRE}}$ | AMSIG | Amplitude control signal from AM buffer from Phase Lock Loop Board. |
| $\overline{\text{SELBAL2}}$ | BOUT2 | Negative Balance Driver output from Output Board. |
| $\overline{\text{SELBAL1}}$ | BOUT1 | Positive Balance Driver output from Output Board. |
| $\overline{\text{SELPA}}$ | PA OUT | Power Amplifier output from Output Board. |

goes low which resets the peak detector. The relay (K7) bypasses the peak detector when the Internal Calibration Network measure dc voltages from the Output Board. Three switches (U8A - U8C) select the inputs to the peak detector. Table 5-12 describes the inputs and the control lines that selects them.

The THD Filter is a Twin Tee Notch filter that receives its input , SIN1, from the Sine Buffer on the Phase Lock Loop Board. The Filter (schematic 1104-00-3335 sheet 6 of 6) consists of the actual filter (U10B) and an rms Detector (U10A). The notch filter has a center frequency of about 10 kHz. The rms Detector provides a dc voltage proportional to the harmonics of the 10 kHz sine wave input.

The Frequency Measurement Section consists of three inputs to the Microprocessor Section; refer to paragraph 5.6.2.

## 6.1 Introduction

This section presents information, which when used with the Verification Procedure (Section 3), the Circuit Description (Section 5), and the Schematic and Assembly Drawings (Section 7), returns the Model 90 to operating condition. This section covers:

Factory Service,
Problem Isolation,
Disassembly and Reassemble - including board removal.

## 6.2 Routine Maintenance

Section 2 of this manual covers routine maintenance of the Model 90.

## 6.3 Factory Service

Wavetek maintains a factory repair department for those customers not possessing the personnel or test equipment to troubleshoot the instrument. If an instrument is returned to the factory for calibration or repair, a detailed description of the problem symptoms should be attached to minimize turnaround time.

Wavetek San Diego, Inc.
9045 Balboa Ave.
San Diego, CA 92123
Telephone: (619) 279-2200
TWX: (910) 335-2007
FAX: (619) 565-9558

Before returning the instrument, call Wavetek's Customer Service department and obtain a Return Authorization Number; Wavetek uses this number to identify your instrument while it is in for repair.

The instrument should be packed according to the instructions in paragraph 2.3 of the *Model 90 Operator's Manual.*

## 6.4 Before Beginning

Before beginning the troubleshooting process, verify that the instrument setup is correct. See section 3 of the *Model 90 Operator's Manual.*

Visually inspect the instrument for physical damage, paragraph 6.6.1.

Check the primary source:

1. Check the primary source.
2. Check the power cord.
3. Verify the primary supply voltage and the units voltage selection match; see paragraph 2.4.1 of the *Model 90 Operator's Manual.*
4. Check the unit's fuse; see paragraph 2.2 of this manual.

## 6.5 Troubleshooting Philosophy

The intent of this section is not to isolates failures to the component level but to give service technicians a set of "tools" that will guide them to the most likely circuit or circuits. From that point, the service technician must turn to the appropriate set of schematics and assembly drawings in the rear of this manual, and together with the circuit description (section 5) isolate the faulty component.

## 6.6 Before Troubleshooting

### 6.6.1 Inspection

Before beginning the troubleshooting procedure, use the following inspection procedures to locate obvious malfunctions with the Model 90.

1. Inspect all external surfaces of Model 90 for physical damage, breakage, loose or dirty contacts, and missing components.
2. Remove top cover, shield, and bottom cover to access components; paragraph 6.9.

**WARNING**

**The Model 90 contains high voltages. After power is removed, discharge capacitors to ground before working inside the instrument to prevent electrical shock.**

CAUTION

Do not disconnect or remove any board assemblies in the Model 90 unless the instrument is unplugged. Some board assemblies contain devices that can be damaged if the board is removed with the power on. Several components, including MOS devices, can be damaged by electrostatic discharge. Use conductive foam and grounding straps when servicing is required around sensitive components. Use care when unplugging ICs from high-grip sockets.

3. Inspect printed circuit board surfaces for discoloration, cracks, breaks, and warping.
4. Inspect printed circuit board conductors for breaks, cracks, cuts, erosion, or looseness.
5. Inspect all assemblies for burnt or loose components.
6. Inspect all chassis-mounted components for looseness, breakage, loose contacts or conductors.
7. Inspect the Model 90 for disconnected, broken, cut, loose, or frayed cables or wires.

### 6.6.2 Test Point Access

Test point access on the vertically mounted boards requires that, during signal tracing, a board be connected to the mother board through special extender cards.

Since only one board can be extended at a time and still allow access to components and test points, the person performing the troubleshooting should review the fault and the fault isolation steps logically to determine a plan that will require the least amount of board removal and reinstallation.

CAUTION

Do not install or remove vertical board assemblies from the mother board with the operating power ON. Damage to components on the assemblies will occur if the assemblies are removed or inserted with operating power on.

CAUTION

Before removing Aux board, disconnect cables which are attached to board through holes in the rear shield.

Test points called out in the following procedures are shown on the assembly drawings and the schematic diagrams for each vertical board and the mother board. Three types of test points are shown. Numbered test points which are actual reference designator components on the board, and numbered test points which are locations on components that have been added as an aid in fault isolation. The final test points are actually pins on ICs and connectors.

Some circuits on the motherboard and the phase lock loop board are shielded by rectangular metal cans soldered to the board traces. Test points located under these shields must be accessed from the solder side of the boards. Do not remove the shields except if repair is required in the shielded area.

### 6.6.3 Board Location

Figure 6-1 shows the location of the board assemblies in the Model 90.

## 6.7 Fault Isolation

This paragraph provides a series of procedures that when followed will point to recommended circuit blocks. Skip those procedures that do not apply to your symptom. Each circuit block reference will contain additional references to the proper Circuit Description paragraphs and Schematic and Assembly drawings. Use the circuit descriptions in conjunction with the schematics to gain a deeper understanding of the circuit block. Table 6-1 lists the recommended equipment necessary to troubleshoot the Model 90.

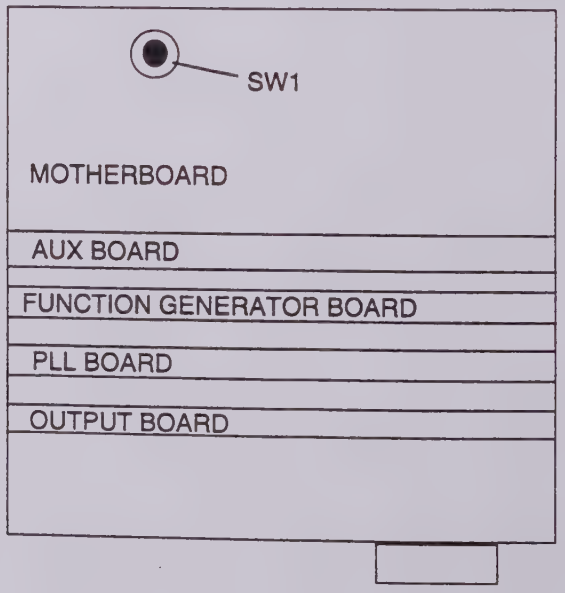



Figure 6-1. Board Locations

Table 6-1. Recommended Equipment

| Equipment | Requirements |
|---|---|
| Scope | Dual trace, 20 MHz Bandwidth |
| Digital Voltmeter | Three Digit Accuracy (minimum). |
| Frequency Counter | >Four Digits of resolution, <±10 ppm accuracy. (Synthesizer and Optional Frequency Reference.) |
| Board Extender Kit | Wavetek part number 1100-00-3411 |

### 6.7.1 Front Panel Not Active

Neither the front panel's display, annunciators, or keyboard operate.

1. Check the primary source; paragraph 6.4.
2. Visually inspect the unit; paragraph 6.6.

Secondary Supplies

1. Remove the top cover (see paragraph 6.9.1 - Top Cover/Shield Removal)
2. Check the unit's secondary supplies using the digital voltmeter. Table 6-2 lists the power supplies, their voltages and tolerances, as well as drawing references. Test Points are located on the Motherboard. All voltages are referenced to analog ground (TP6). Also check the power supplies distribution system.

Power Supplies check OK.

1. Check the Microprocessor Section: Schematic 1104-00-3395 Sheet 3 of 10, Assembly drawing 1101-00-3395 sheet 1 of 3. For a description of the Microprocessor Section's circuits, refer to paragraph 5.6.2.
2. Check the microprocessor section: paragraph 6.8.16.

   *HINTS*

   Check the supply voltages to the circuits within the Microprocessor Section.

   Using the scope, check the control and data lines. Most line should be "moving". Lines stuck high or low could identify a defective device.
3. If the key pad and display still do not operate, check the front panel input decoder, U4. Refer to schematic 0103-00-3001 sheet 3 of 3, assembly drawing 1101-00-3322 sheet 1 of 2, circuit description paragraph 5.7.4.5.

### 6.7.2 Front Panel Not Active Keyboard Does Not Work

1. Refer to schematic 1104-00-3322, assembly drawing 1101-00-3322 sheet 1 of 2, and circuit description paragraph 5.6.4.5 - Keyboard.
2. Check the supply voltages to the circuits within the Keyboard.

   Using the scope, check the control and data lines. Most lines should be "moving". Lines stuck high or low could identify a defective device.

### 6.7.3 Front Panel Not Active - Display Does Not Work

1. Refer to schematic 1104-00-3322, assembly drawing 1101-00-3322 sheet 1 of 2, and circuit description paragraph 5.6.4.5 - Display.
2. Check the supply voltages to the circuits within the Display.

   Using the scope, check the control and data lines. Most lines should be "moving". Lines stuck high or low could identify a defective device.

### 6.7.4 Front Panel Not Active - Annunciators Do Not Work

1. Refer to schematic 1104-00-3322, assembly drawing 1101-00-3322 sheet 1 of 2, and circuit description paragraph 5.6.4.5 - Annunciator Circuit.
2. Check the supply voltages to the circuits within the Display.

   Using the scope, check the control and data lines. Most lines should be "moving". Lines stuck high or low could identify a defective device.

### 6.7.5 Self Test and Self Test Error Messages

When power is first applied, the Model 90 performs Self Test. Self test checks the unit's internal battery,

Table 6-2 Power Supply Test Points

| Test Point | Supply Voltage | Tolerance | Schematic Drawing | Assembly Drawing |
|---|---|---|---|---|
| JMP 4 | +12VDC | ±0.2 Vdc | 1104-00-3395 Sheet 8 of 10 | 1101-00-3396 Sheet 1 of 3 |
| JMP 5 | -12VDC | ±0.2 Vdc | 1104-00-3395 Sheet 8 of 10 | 1101-00-3396 Sheet 1 of 3 |
| JMP 6 | +5V | ±0.2 Vdc | 1104-00-3395 Sheet 8 of 10 | 1101-00-3396 Sheet 1 of 3 |
| TP14 | +24 VDC | ±0.2 Vdc | 1104-00-3395 Sheet 9 of 10 | 1101-00-3396 Sheet 1 of 3 |
| TP15 | -24VDC | ±0.2 Vdc | 1104-00-3395 Sheet 9 of 10 | 1101-00-3396 Sheet 1 of 3 |

Motherboard memory, and storage memory. Failure of any of the tests will cause the Model 90 to display an error message. Table 6-3 defines the error messages. If Self Test is successful, the Model 90 will display "Wavetek Model 90".

### 6.7.6 Autocal and Autocal Error Messages

The Model 90 contains a powerful fault isolation tool: Autocal. Autocal measures numerous "test points" in the Model 90. It compares these measurements against either a frequency standard or voltage standard. Autocal attempts to make correction for any deviations. But if Autocal can not bring the measurement within limits, the Model 90 produces an error message. The Model 90 runs Autocal until it hits its first error. Then it stops until the error is fixed by either performing the Calibration procedure, section 4, or isolating and fixing the problem. Continue running Autocal until all problems have been identified and fixed.

To Autocal the Model 90, perform the following steps. Autocal requires no external test equipment. In fact, test equipment should not be connected to the Model 90 input connectors, otherwise the Autocal could alter the calibration of the instrument. Also, disconnect all outputs from the instrument otherwise the sudden changes in the instrument's output waveforms could damage external equipment.

1. Turn on the Model 90 and allow it to warm up for 20 minutes. Pressing the CALIBRATE key during the 20 minute warm up time displays the count-down time, after the 20 minutes the Model 90 begins Autocal. Pressing any other key during the count down aborts Autocal and returns the instrument to normal operation.

   REMEMBER

   Remove all input and output connections to the Model 90 before pressing Autocal.

2. After a 20 minute warm up, press the SHIFT and CALIBRATE key and allow the unit time to complete the Autocal cycle. While running Autocal, the Model 90 displays "CALIBRATING". When completed successfully, the Model 90 displays "AUTOCALIBRATED". Then the unit returns to its last operational setup. If the Autocal fails the Model 90 displays an error message which identifies the parameter - ERR (*Keyword*); for example ERR VSINCAL. If this occurs occasionally, try to Autocal the unit again. Note the error keywords and report the errors when the unit is returned for scheduled maintenance.
3. If repeating the Autocal procedure a second time returns the same message, try the following steps before beginning block isolation. This procedure erases the calibration values stored in the Model 90 memory and replaces the calibration values with nominal calibration values.
   - A. After a 20 minute warm up, press the internal calibration switch while pressing the CALIBRATE key (paragraph 4.3, Step 2 Initial Steps).
   - B. Press the PARAM RESET key to load the nominal calibration values of the Model 90.
   - C. Press the CALIBRATE key to return to normal operation.

D. Perform the Calibration Procedure (paragraph 4.3).

Following is a listing of the Autocal error messages. Included is a brief description of the Autocal step. In addition, each step contains Pass/Fail instructions.

VCG0 This check adjusts out frequency shift error in the function generator. The test sets the generator to 200 Hz on the 200 kHz range and using the internal calibration network adjusts out 1000:1 frequency errors (<0.7 Hz deviation).

**Table 6-3. Self Test Error Messages**

| Display | Probable Cause | Corrective Action |
|---|---|---|
| Err xxxxxxxxx | Improper self-check/unit | Press POWER key OFF and then ON. If identical failure error is displayed, refer to paragraph 6.7.6. If "WAVETEK MODEL 90" is displayed, the unit is operational. |
| Low batt x.xxx v | Internal battery voltage low. | Unit is available for immediate operation. Refer to paragraph 2.3 for battery replacement. |
| Cal Required | Internal battery dead. | Unit has lost its calibration data but can be used after performing and passing AutoCal. Instrument may not meet all specifications. |

Passes: Verifies the function generator operates correctly. No message will be displayed and Autocal moves to the next step.
Fail: If the unit displays the VCGO message, it means the Function Generator may not be working correctly. Use the procedure in paragraph 6.8.1 to isolate the faulty circuit.

VFREQ0 This check zeros the VCG summing amplifier with the VFREQ input connected. It also zeros the Function Generator board's Autocal circuit. Test requires the VSUM voltage be <20 mV of analog ground.
Passes: Verifies the VCG Summing Amplifier and Autocalibration circuit operates correctly. No message will be displayed and Autocal moves to the next step.
Fail: If the unit displays the VFREQ0 message, it means the VCG Summing Amplifier or Autocal circuit may not be working correctly. Use the procedure in paragraph 6.8.1 to check the VCG Summing Amplifier. Use paragraph 6.8.9 to check the function generator's Autocal circuit.

VFREQ0 SCL This check zeros the VCG Summing amplifier with the VFREQ input disconnected. It also zeros the Function Generator board's Autocal circuit. Test requires the VSUM voltage be <10 mV of analog ground.
Passes: Verifies the VCG summing Amplifier and Autocalibration circuit operates correctly. No message will be displayed and Autocal moves to the next step.
Fail: If the unit displays the VFREQ0 message, it means the VCG summing amplifier or Autocal circuit may not be working correctly. Use the procedure in paragraph 6.8.1 to check the VCG summing amplifier.

S+VCGOFF This check zeros (<20 mV) the positive symmetry control relative to the analog ground.
Passes: Verifies the positive symmetry control works. No message will be displayed and Autocal moves to the next step.
Fails: Check the Symmetry Control, paragraph 6.8.3.

S–VCGOFF This check zeros (<20 mV) the negative symmetry control relative to the analog ground.
Passes: Verifies the negative symmetry control works. No message will be displayed and Autocal moves to the next step.
Fails: Check the Symmetry Control, paragraph 6.8.3.

VTRIBAL This check zeros (<59 mV) the triangle buffer, TRIBAL, relative to analog ground, TRICOM.
Passes: Verifies the negative symmetry control works. No message will be displayed and Autocal moves to the next step..
Fails: Check the Triangle Buffer and Comparator, paragraph 6.8.2.

SYMM50PCT This check sets the symmetry control to 50%, symmetry off, and adjusts for 50% ±0.03% symmetry at 201 Hz on the 200 kHz.
Passes: Verifies the symmetry control and current sources work. No message will be displayed and Autocal moves to the next step.
Fails: Check the symmetry control (paragraph 6.8.3) and current sources (paragraph 6.8.4).

+VCGOFF This check turns on the symmetry, sets the symmetry to 50%, and adjusts the symmetry to 50%.
Passes: Verifies the symmetry control and current sources work. No message will be displayed and Autocal moves to the next step.
Fails: Check the symmetry control, paragraph 6.8.3.

SWPLENGTH This check sets VSLEN (sweep length) DAC reference input and adjusts the sweep DAC to a specified frequency.
Passes: Verifies the sweep generator works. No message will be displayed and Autocal moves to the next step.
Fails: Check the Sweep Generator, paragraph 6.8.10.

SCALE This check sets VFREQ input to the VCG summing amplifier to a level that when the Scale switch is open causes the function generator to produces a 20 kHz signal. The internal calibration network adjusts VFREQ to 20 kHz ±1Hz

Passes: Verifies the frequency accuracy at 1000:1 on the 20 MHz range. No message will be displayed and Autocal moves to the next step.
Fails: Check the function generator, paragraph 6.8.1. Also check the DAC Sample and Hold Network, paragraph 6.8.17.

TOFR7 This check sets the function generator to the 200 kHz range. The internal calibration network measures and adjusts VFREQ to 200 kHz ±10 Hz.
Passes: Verifies the frequency accuracy at the top of the 200 kHz range. No message will be displayed and Autocal moves to the next step.
Fails: Check Frequency Range Switch Circuit, paragraph 6.8.7. Also check the function generator, paragraph 6.8.1.

TOFR6 This check sets the function generator to the 20 kHz range. The internal calibration network measures and adjusts VFREQ to 20 kHz ±1Hz.
Passes: Verifies the frequency accuracy at the top of the 20 kHz range. No message will be displayed and Autocal moves to the next step.
Fails: Check Frequency Range Switch Circuit, paragraph 6.8.7. Also check the function generator, paragraph 6.8.1.

TOFR5 This check sets the function generator to the 2kHz range. The internal calibration network measures and adjusts VFREQ to 200 kHz ±0.15 Hz.
Passes: Verifies the frequency accuracy at the top of the 2kHz range. No message will be displayed and Autocal moves to the next step.
Fails: Check Frequency Range Switch Circuit, paragraph 6.8.7. Also check the function generator, paragraph 6.8.1.

TOFR4 This check sets the function generator to the 200 Hz range. The internal calibration network measures and adjusts VFREQ to 200 Hz ±0.01 Hz.
Passes: Verifies the frequency accuracy at the top of the 200 Hz range, and verifies the operation of the capacitance multiplier. No message will be displayed and Autocal moves to the next step.
Fails: Check the capacitance multiplier, paragraph 6.8.8. Also check the function generator, paragraph 6.8.1.

TOFR3 This check sets the function generator to the 20 Hz range. The internal calibration network measures and adjusts VFREQ to 20 Hz ±0.02 Hz.
Passes: Verifies the frequency accuracy at the top of the 20 Hz range, and verifies the operation of the capacitance multiplier. No message will be displayed and Autocal moves to the next step.
Fails: Check the capacitance multiplier, paragraph 6.8.8. Also check the function generator, paragraph 6.8.1.

COMP9+ This check sets the function generator to 20 MHz range. Then sets VFREQ to 2MHz. Next the VFREQ value is set for 20 MHz, and the high frequency DAC adjusted for 20 MHz. The cycle repeats for up to 20 iterations.
Passes: Verifies the 20 MHz range 10:1 frequency linearity. No message will be displayed and Autocal moves to the next step.
Fails: Check the high frequency compensation circuit, paragraph 6.8.6. Also check the function generator, paragraph 6.8.1.

COMP8+ This check sets the function generator to 2MHz range. Then it sets VFREQ to 200 kHz. Next the VFREQ value is set for 2MHz, and the high frequency DAC adjusted for 2MHz. The cycle repeats for up to 20 iterations.
Passes: Verifies the 2MHz range 10:1 frequency linearity. No message will be displayed and Autocal moves to the next step.
Fails: Check the high frequency compensation circuit, paragraph 6.8.6. Also check the function generator, paragraph 6.8.1.

FINDNOTCH This check sets the function generator to a 10 kHz sine wave. Then using the notch filter and internal calibration network adjusts the frequency (VFREQ) to 10 kHz.
Passes: Verifies the sine convertor and buffer, variable supply, and notch filter operates correctly. No message will be displayed and Autocal moves to the next step.

Fails: Check the Sine Buffer, Sine Converter, and Variable Supply. See paragraph 6.8.11.

OFSTZERO This check sets the function to dc and the offset voltage to 0Vdc. Then measuring the power amplifier output with the internal calibration network, adjusts the offset (VOFST) to <9 mV.
Passes: Verifies the operation of the power amplifier. No message will be displayed and Autocal moves to the next step.
Fails: Check the power amplifier; see paragraph 6.8.13. Also, check the DAC Sample and Hold Network, paragraph 6.8.17.

OFSTGAIN This check sets the function to dc and the offset voltage to 5Vdc. Then measuring the power amplifier output with the internal calibration network, adjusts the offset gain (VOFST) to +5Vdc ±9mV.
Passes: Verifies the operation of the power amplifier. No message will be displayed and Autocal moves to the next step.
Fails: Check the power amplifier; see paragraph 6.8.13. Also check the DAC Sample and Hold Network, paragraph 6.8.17.

BALOFFST This check sets the function to dc and the offset voltage to 0Vdc. The internal calibration network measures the two balanced outputs and adjusts the offset voltage (VOFST) so the difference between the two outputs is <3 mVdc.
Passes: Verifies the operation of the balanced drivers. No message will be displayed and Autocal moves to the next step.
Fails: Check the balanced drivers, paragraph 6.8.13.

SINEAMPL This check sets the function to sine wave and using the peak detector, measures the peak to peak amplitude of the sine wave, and adjust amplifier output via VAMCAL to 20 ±0.03 Vpp.
Passes: Verifies the operation of the function selector, preamplifier and multiplier, and AM buffer. No message will be displayed and Autocal moves to the next step.
Fails: Check the function selector (paragraph 6.8.13), preamplifier/multiplier (paragraph 6.8.13), and AM buffer (paragraph 6.8.13).

TRIAMPL This check sets the function to triangle wave and using the peak detector, measures the peak to peak amplitude of the triangle wave, and adjust amplifier output via VAMCAL to 20 ±0.03 Vpp.
Passes: Verifies the operation of the function selector, preamplifier and multiplier, and AM buffer. No message will be displayed and Autocal moves to the next step.
Fails: Check the function selector (paragraph 6.8.13), preamplifier/multiplier (paragraph 6.8.13), and AM buffer (paragraph 6.8.13).

SQURAMPL This check sets the function to square wave and using the peak detector, measures the peak to peak amplitude of the square wave, and adjust amplifier output via VAMCAL to 20 ±0.03 Vpp.
Passes: Verifies the operation of the function selector, preamplifier and multiplier, and AM buffer. No message will be displayed and Autocal moves to the next step.
Fails: Check the function selector (paragraph 6.8.13), preamplifier/multiplier (paragraph 6.8.13), and AM buffer (paragraph 6.8.13).

BALAMPL This check adjusts the balanced output amplitude to 20 ±0.03 Vpp by measuring the balanced driver output with the peak detector and varying VAMCAL.
Passes: Verifies the operation of the balanced drivers. No message will be displayed and Autocal moves to the next step.
Fails: Check the balanced drivers, paragraph 6.8.13. Also, check the -20 dB Attenuator, paragraph 6.8.13.

VSINCAL This check sets the function generator to a 10 kHz sine wave. Then using the notch filter and internal calibration network adjusts the sine wave harmonic distortion.
Passes: Verifies the sine convertor and buffer, variable supply, and notch filter operates correctly. No message will be

displayed and Autocal moves to the next step if the optional high voltage .amplifier is installed. If the high voltage amplifier is not installed, the Autocal cycle is completed.
Fails: Check the Sine Buffer, Sine Converter, and Variable Supply. See paragraph 6.8.11.

HI-VGAIN This check adjusts the gain of the high voltage amplifier.
Passes: Verifies the high voltage amplifier operates correctly. No message will be displayed and Autocal moves to the next step.
Fails: Check the high voltage amplifier; paragraph 6.8.14.

HI-VOFF1 This check adjusts offset errors in the high voltage amplifier's 0, 40, and 60 dB attenuators.
Passes: Verifies the operation of the 0, 40, and 60 dB attenuators. No message will be displayed and Autocal moves to the next step.
Fails: Check the high voltage amplifier's 0, 40, and 60 dB attenuators, paragraph 6.8.14.

HI-VOFF2 The check adjusts offset error in the high voltage amplifier's 20 and 80 dB attenuators.
Passes: Verifies the operation of the 20, and 80 dB attenuators. This concludes the Autocal cycle.
Fails: Check the high voltage amplifier's 20, and 80 dB attenuators, paragraph 6.8.14.

## 6.8 Block Isolation

The following procedures provide a method of isolating faulty circuit blocks. Most steps use test points; see paragraph 6.6.2.

### 6.8.1 Function Generator

Refer to the function generator assembly drawing (1101-00-3342) and schematic (1104-00-3342 sheets 2 through 7) in section 7 of this manual. Also, refer to paragraph 5.2 of this manual. Reset the unit by pressing SHIFT and RESET ALL keys.

1. First check the function generator board's power input. Schematic 1104-00-3342 sheet 1.

| | |
|---|---|
| TP20 | +5 Vdc |
| TP23 | -12 Vdc |
| TP25 | +24 Vdc |
| TP26 | -24 Vdc |

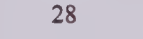
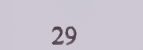
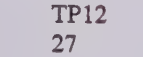
2. Check the following test points which will step you forward through the function generator. If the value at a test point is incorrect, isolate and repair the fault of the circuit between the good and bad test points.

| | | |
|---|---|---|
| 22 | VLOOP | Locked: +0.1 Vdc.<br>Unlocked: -0.5 Vdc. |
| TP2 | VSUM | -2 Vdc |
| TP4 | -FCV | -4 Vdc. |
| TP3 | +FCV | +4 Vdc |
| U22A-1 | +COMP | ≈+2.6 Vdc |
| U22B-7 | -COMP | ≈-2.6 Vdc |
| TP6 | VI+ | +17 Vdc. |
| TP7 | VI- | -17 Vdc. |
| TP9 | TRINODE | 2.5 Vpp Triangle @ 1kHz. |
| TP12 | TRIOUT | 2.5 Vpp triangle @1kHz. |
| TP15 | SQWAVE | 2.25 Vpp square @ 1kHz. |

### 6.8.2 Triangle Buffer/Comparator

Refer to the function generator assembly drawing (1101-00-3342) and schematic (1104-00-3342 sheets 6 and 7) in section 7 of this manual. Also, refer to paragraph 5.2.2 - Comparator and Triangle Buffer. Reset the unit by pressing SHIFT and RESET ALL keys.

1. First isolate the triangle buffer and comparator circuits using paragraph 6.8.1.
2. Check the following test points which will step you through the triangle buffer and comparator. If the value at a test point is incorrect, isolate and repair the fault of the circuit between the good and bad test points.

| | | |
|---|---|---|
| 28 | ISWITCH+ |  3.5 Vpp @ 1kHz. |
| 29 | ISWITCH– |  3.5 Vpp @ 1kHz. |
| TP9 | TRINODE | 2.5 Vpp Triangle @ 1kHz |
| TP12 | TRIOUT | 2.5 Vpp Triangle @ 1kHz. |
| 27 | TRI/SQR |  2.5 Vpp @ 1kHz. |
| 18 | SQ1 | 1Vpp square offset +8 Vdc @ 1kHz. |
| 19 | SQ2 | 4Vpp Square @ 1kHz. |
| TP15 | SQWAVE | 2.5 Vpp Square @ 1kHz. |
| TP13 | REFSQR | 2.5 Vpp square @ 1kHz. |

### 6.8.3 Symmetry Control

Refer to the function generator assembly drawing (1101-00-3342) and schematic (1104-00-3342 sheet 3) in section 7 of this manual. Also, refer to paragraph 5.2.4. Reset the unit by pressing SHIFT and RESET ALL keys.

1. First isolate the symmetry control circuit using paragraph 6.8.1.

2. Check the following test points which will step you through the symmetry control circuit. If the value at a test point is incorrect, isolate and repair the fault of the circuit between the good and bad test points.

| | | |
|---|---|---|
| TP2 | VSUM | -2 Vdc. |
| 21 | DAC reference | -6 Vdc |
| TP3 | +FCV | +4 Vdc |
| TP4 | -FCV | -4 Vdc |

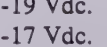
3. Verify the data line "wiggle". U12, pins 9, 10, 11, 12, 13, 14, 15, and 16. U17, pins 9, 10, 11, 12, 13, 14, 15, and 16. The following table identifies the enable DAC.

| | DS1 | DS2 | A/B |
|---|---|---|---|
| Pin # | 19 | 20 | 17 |
| U7C Enabled | 1 | 0 | 1 |
| U7D Enabled | 1 | 0 | 0 |
| U12B Enabled | 0 | 1 | 0 |
| U12A Enabled | 0 | 1 | 1 |

### 6.8.4 VCG Current Sources

Refer to the function generator assembly drawing (1101-00-3342) and schematic (1104-00-3342 sheet 3) in section 7 of this manual. Also, refer to paragraph 5.2.2.2, VCG Current Sources. Reset the unit by pressing SHIFT and RESET ALL keys.

1. First isolate the symmetry control circuit using paragraph 6.8.1.
2. Check the following test points which will step you through the symmetry control circuit. If the value at a test point is incorrect, isolate and repair the fault of the circuit between the good and bad test points.

| | | |
|---|---|---|
| TP3 | +FCV | +4 Vdc. |
| TP5 | +VCG | +19 Vdc. |
| TP6 | VI+ | +17 Vdc. |
| 28 | ISWITCH+ | 3.5 Vpp @1kHz. |
| TP4 | -FCV | -4 Vdc. |
| TP8 | -VCG | -19 Vdc. |
| TP7 | -VI | -17 Vdc. |
| 29 | ISWITCH- |  3.5 Vpp @ 1kHz. |

### 6.8.5 Trigger Baseline Compensation

Refer to the function generator assembly drawing (1101-00-3342) and schematic (1104-00-3342 sheet 4) in section 7 of this manual. Also, refer to paragraph 5.2.5, Trigger Baseline Compensation. Reset the unit by pressing SHIFT and RESET ALL keys.

1. First isolate the symmetry control circuit using paragraph 6.8.1. Note, if the generator does not run, check this circuit.
2. Check the following test points which will step you through the trigger baseline compensation circuit. If the value at a test point is incorrect, isolate and repair the fault of the circuit between the good and bad test points.

| | | |
|---|---|---|
| U19-3 | VSOURCE | +17 Vdc |
| TP5 | +VCG | +19 Vdc |
| TP8 | -VCG | -19 Vdc |
| 17 | RUN | +4 Vdc for continuous. 0Vdc off. |
| TP9 | TRINODE | 2.5 Vpp |

### 6.8.6 High Frequency Compensation

Refer to the function generator assembly drawing (1101-00-3342) and schematic (1104-00-3342 sheet 4) in section 7 of this manual. Also, refer to paragraph 5.2.5. Reset the unit by pressing SHIFT and RESET ALL keys.

1. First isolate the symmetry control circuit using paragraph 6.8.1.
2. Check the following test points which will step you through the high frequency circuit. If the value at a test point is incorrect, isolate and repair the fault of the circuit between the good and bad test points.

| | | |
|---|---|---|
| TP3 | +FCV | +4 Vdc |
| U12C-2 | Vref | -5 Vdc |
| U22A-1 | +COMP | ≈+2.6 Vdc |
| TP4 | -FCV | -4 Vdc |
| U12A-8 | Vref | +5 Vdc |
| U22B-7 | -COMP | ≈-2.6 Vdc |

3. Verify the data lines "wiggle". U12, pins 9, 10, 11, 12, 13, 14, 15,. The following material identifies the enabled DAC.

| | DS1 | DS2 | A/B |
|---|---|---|---|
| Pin # | 19 | 20 | 17 |
| U12C Enabled | 1 | 0 | 1 |
| U12D Enabled | 1 | 0 | 0 |

### 6.8.7 Frequency Range Switches

Refer to the function generator assembly drawing (1101-00-3342) and schematic (1104-00-3342 sheet 5) in section 7 of this manual. Also, refer to paragraph 5.2.2.3, Frequency Range Capacitors and Ranges. Reset the unit by pressing SHIFT and RESET ALL keys.

1. First isolate the frequency range capacitor circuit using paragraph 6.8.1.
2. Check the test point, TP9 - TRINODE, for a 2.5 Vpp triangle @ 1kHz.
3. Verify the following frequency range control lines are low: $\overline{FR5}$, $\overline{FR6}$, $\overline{FR7}$ $\overline{FR8}$. Note, in the default

settings, the 2kHz to 200 Hz range is selected. For all frequencies above 200 Hz, refer to the control lines and capacitors listed in table 6-4.

### 6.8.8 Capacitance Multiplier

Refer to the function generator assembly drawing (1101-00-3342) and schematic (1104-00-3342 sheet 6) in section 7 of this manual. Also, refer to paragraph 5.2.2.4, Capacitance Multiplier. Reset the unit by pressing SHIFT and RESET ALL keys.

1. First verify the function generator operates correctly using paragraph 6.8.1.
2. Change the unit's frequency to 100 Hz. Check the test point, TP11 - CAP MULT, for ∿∿ 5Vpp @ 100 Hz.

Also verify the 2KHz range capacitor is selected: 0.52219 µF - C52, C53,C55,C57, C58, C67 (≤$\overline{FR5}$, ≤$\overline{FR6}$, ≤$\overline{FR7}$ ≤$\overline{FR8}$)

For frequencies below 200 Hz, refer to the control lines and capacitors listed in table 6-5.

### 6.8.9 Function Generator Autocalibration

Refer to the function generator assembly drawing (1101-00-3342) and schematic (1104-00-3342 sheet 4) in section 7 of this manual. Also, refer to paragraph 5.6.6. This circuit is active only when Autocal is being performed. The following describes the function generator Autocal mux controls.

| A0 | A1 | A2 | Name |
|---|---|---|---|
| U28 Pin | 1 | 16 | 15 |
| 0 | 0 | 0 | Ground |
| 1 | 0 | 0 | VSUM |
| 0 | 1 | 0 | +FCV |
| 1 | 1 | 0 | -FCV |
| 0 | 0 | 1 | +COMP |
| 1 | 0 | 1 | -COMP |
| 0 | 1 | 1 | TRIBAL |
| 1 | 1 | 1 | TRICOM |

### 6.8.10 Sweep Generator

Refer to the function generator assembly drawing (1101-00-3342) and schematic (1104-00-3342 sheet 2) in section 7 of this manual. Also, refer to paragraph 5.4.3 . Reset the unit by pressing SHIFT and RESET ALL keys.

1. First verify the function generator operates correctly using paragraph 6.8.1.
2. Select the sweep mode.
3. Check the following test points which will step you through the sweep generator. If the value at a test point is incorrect, isolate and repair the fault of the circuit between the good and bad test points.

| | | |
|---|---|---|
| J6-39 | VSLEN | |
| U7A-8 | Vref | -3 x (VSLEN) |
| U8-6 | Sweep Out | Approx. 3 x (VSLEN) |

**Table 6-4. Frequency Range Capacitors**

| Range | Capacitors | Control |
|---|---|---|
| 20 - 2 MHz | 50 pF - (15 pF + Stray) C67 | None |
| 2MHz - 200 kHz | 490 pF - C57, C58, C67 | ≤$\overline{FR8}$ |
| 200 kHz - 20 kHz | 0.00519 µF - C55,C57, C58, C67 | ≤$\overline{FR7}$, ≤$\overline{FR8}$ |
| 20 kHz - 2kHz | 0.05219 µF - C53,C55,C57, C58, C67 | ≤$\overline{FR6}$, ≤$\overline{FR7}$, ≤$\overline{FR8}$ |
| 2kHz - 200 Hz | 0.52219 µF - C52, C53,C55,C57, C58, C67 | ≤$\overline{FR5}$, ≤$\overline{FR6}$, ≤$\overline{FR7}$ ≤$\overline{FR8}$ |

**Table 6-5 Capacitance Multiplier Ranges**

| Range | Resistors | Control |
|---|---|---|
| 200 Hz - 20 Hz | 10 kΩ - R67 | $\overline{FR4}$ |
| 20Hz - 2Hz | 110 kΩ - R67, R68 | $\overline{FR4}$, $\overline{FR3}$ |
| 2Hz - 200 mHz | 1.11 MΩ - R67, R68, R69 | $\overline{FR4}$, $\overline{FR3}$, $\overline{FR2}$ |
| 200 mHz - 20 mHz | 11.11 MΩ - R67, R68, R69, R71 | All high |
| 20 mHz - 2mHz | See Note | |

*NOTE*

*The Model 90 does not switch to the 20 mHz range. It actually keeps the same range capacitors as the 200 mHz range, but it decreases the input to the VCG Summing Amplifier by 1/10th effectively dropping down a decade range by switching in,* $\overline{SCALE}$ *an additional input resistor (R8) in series with the VFREQ input.*

Check the sweep DAC.

| | DS1 | DS2 | A/B |
|---|---|---|---|
| Pin # | 19 | 20 | 17 |
| U7A Enabled | 0 | 1 | 1 |

Verify the DAC data lines (U7 - 9, 10, 11, 12, 13, 14,15, and 16) step from 00000000 to 11111111.

4. Check the Sweep Out (Ramp) generator test points.

| | | |
|---|---|---|
| U7A-21 | Vref | -6 Vdc |
| SWEEP OUT Connector | | 0 to +5V linear ramp. |

Check the Sweep Out DAC.

| | DS1 | DS2 | A/B |
|---|---|---|---|
| Pin # | 19 | 20 | 17 |
| U7A Enabled | 0 | 1 | 0 |

Verify the DAC data lines (U7 - 9, 10, 11, 12, 13, 14, 15, and 16) step from 00000000 to 11111111.

### 6.8.11 Sine Convertor, Buffer, and Variable Supply

Refer to the Phase Lock Loop assembly drawing (1101-00-3342) and schematic (1104-00-3341 sheets 5 and 6) in section 7 of this manual. Reset the unit by pressing SHIFT and RESET ALL keys.

1. First verify the function generator operates correctly using paragraph 6.8.1.
2. Check the following test points which will step you through the sine wave circuits. If the value at a test point is incorrect, isolate and repair the fault of the circuit between the good and bad test points.

| | | |
|---|---|---|
| 25 | TRISIG | 2.5 Vpp triangle @ 1kHz. |
| 27 | SINSIG | 2.5 Vpp triangle @ 1kHz. |
| TP13 | SINCO | 0.6 Vpp sine @ 1kHz. |
| TP10 | SIN | 2 Vpp sine @ 1kHz. |
| TP14 | +12VADJ | Approximately +12 Vdc. |
| TP15 | -12VADJ | Approximately -12 Vdc. |

### 6.8.12 Mode Control and Burst Counter

Refer to the Aux board assembly drawing (1101-00-3386) and schematic (1104-00-3386 sheet 1) in section 7 of this manual. Reset the unit by pressing SHIFT and RESET ALL keys.

1. Check the test point, TP3 - RUN, +4 Vdc.
2. Select the Triggered Mode. Check the test point, TP3 - RUN, 0Vdc.
   Press the Man Trig key on the front panel. TP3 toggles to +4 Vdc and returns to 0Vdc.
3. Refer to paragraph 5.5 for a detailed description of the mode control and burst counter circuits.

### 6.8.13 Output Section

This procedure steps through each block of the output block. Refer to the Output board assembly drawing (1101-00-3335), Motherboard assembly drawing (1101-00-3395), Output board schematic (1104-00-3335) , and Motherboard schematic (1104-00-3395 sheet 7) in section 7 of this manual. Also, refer to the output section circuit description, paragraph 5.3.

Check the following test points which will step you through the output section. If the value at a test point is incorrect, isolate and repair the fault of the circuit between the good and bad test points.

1. Square Shaper (schematic 1104-00-3335 sheet 2). Reset the unit by pressing SHIFT and RESET ALL keys.

| | | |
|---|---|---|
| Q2 base | SQRON | =0Vdc |

Select Square function.

| | | |
|---|---|---|
| Q2 base | SQRON | >+2.5Vdc |
| JMP1 | SQWAVE | 2.25 Vpp square @ 1kHz. |
| TP1 | 2V P-P SQUARE | 1Vpp square @ 1kHz. |

2. Function Selector (schematic 1104-00-3335 sheet 3). Reset the unit by pressing SHIFT and RESET ALL keys.

| | | |
|---|---|---|
| 19 | PREAMPIN | 1Vpp square @ 1kHz. |

Select Sine function

| | | |
|---|---|---|
| 19 | PREAMPIN | 1Vpp sine @ 1kHz. |

Select Triangle function

| | | |
|---|---|---|
| 19 | PREAMPIN | 1Vpp triangle @ 1kHz. |

On the Phase Lock Loop Board, (schematic 1104-00-3341 sheet 4),

| | | |
|---|---|---|
| 26 | TRIOUT | 1.5 Vpp triangle @ 1kHz. |

3. Preamplifier and Multiplier (schematic 1104-00-3335 sheet 3). Reset the unit by pressing SHIFT and RESET ALL keys.

| | | |
|---|---|---|
| 19 | PREAMPIN | 1Vpp sine @ 1kHz. |
| TP11 | +6V | +6 Vdc |
| TP12 | -6V | -6 Vdc |
| TP2 | PREOUT | 1.5 Vpp sine @ 1kHz offset +4 Vdc. |

4. AM Summing Amplifier (schematic 1104-00-3341 sheet 6). Reset the unit by pressing SHIFT and RESET ALL keys.

| | | |
|---|---|---|
| 16 | VAMCAL | Approximately 1.55 Vdc. |
| TP12 | AMSIG | -1.5 Vdc. |

5. Power Amplifier (schematic 1104-00-3335 sheet 4). Reset the unit by pressing SHIFT and RESET ALL keys.

| | | |
|---|---|---|
| TP2 | PREOUT | 1.5 Vpp sine @ 1kHz offset +4 Vdc. |
| 17 | +22V | +22 Vdc |
| 16 | -22V | -22 Vdc |
| TP4 | PA_OUT | 8Vpp sine @ 1kHz. |

6. -20 dB Attenuator (schematic 1104-00-3335 sheet 5). Reset the unit by pressing SHIFT and RESET ALL keys.

| | | |
|---|---|---|
| TP4 | PA_OUT | 8Vpp sine @ 1kHz. |
| J11-1 | UBOUT | 5Vpp sine into 50Ω (10 Vpp unterminated). |

7. Unbalanced Output Attenuator Network and Impedance Control (schematic 1104-00-3395 sheet 7). Reset the unit by pressing SHIFT and RESET ALL keys. Turn the Output On.

| | | |
|---|---|---|
| P11-1 | UBOUT | 5Vpp sine into 50Ω (10 Vpp unterminated). |
| Unbalanced Output connector | | 5Vpp sine into 50Ω (10 Vpp unterminated). |

8. Balanced Drivers (schematic 1104-00-3335 sheet 5). Reset the unit by pressing SHIFT and RESET ALL keys. Select the 600Ω Balanced Output . Turn the output On.

| | | |
|---|---|---|
| 18 | Bal In | 5Vpp sine @ 1kHz. |
| TP6 | BOUT2 | 5Vpp sine @ 1kHz. |
| TP7 | BOUT1 | 5Vpp sine @ 1kHz. |

9. Balanced Output Attenuator Network and Impedance Control (schematic 1104-00-3395 sheet 7). Reset the unit by pressing SHIFT and RESET ALL keys. Select the 600Ω Balanced Output. Turn the output On.

On the Output board, check:

| | | |
|---|---|---|
| TP6 | BOUT2 | 5Vpp sine @ 1kHz. |
| TP7 | BOUT1 | 5Vpp sine @ 1kHz. |

On the Motherboard, check:

| | | |
|---|---|---|
| J21 | BAL OUT (-) | 5Vpp sine terminated. |
| J20 | BAL OUT (+) | 5Vpp sine terminated. |

### 6.8.14 Option 002 High Voltage Output Amplifier

This procedure steps through each block of the high voltage output. Refer to the Auxiliary board assembly drawing (1101-00-3386) and Auxiliary board schematic (1104-00-3386 sheet 3) in section 7 of this manual. Also, refer to the high voltage output circuit description, paragraph 5.3.9. Reset the unit by pressing SHIFT and RESET ALL keys. Select the High Voltage Output and set the amplitude to 40 Vpp; see paragraph 3.5.6.1 of the Model 90 Operator's Manual.

Check following test points on the high voltage output circuit. If the value at a test point is incorrect, isolate and repair the fault of the circuit between the good and bad test points.

| | | |
|---|---|---|
| P36 | FUNC_IN | 10 Vpp sine @ 1kHz. |
| TP8 | | 10 Vpp sine @ 1kHz. |
| TP9 | 20 dB Atten | 1Vpp sine @ 1kHz. |
| TP10 | HI V OUT | 40 Vpp sine @ 1kHz. |
| P32 | HI VOLT OUT | 40 Vpp sine @ 1kHz. |

Check the 40/60 dB attenuator: TP11.

20 dB, Amplitude @ 300 mVpp 300 Vpp sine @ 1kHz.

60 dB, Amplitude @ 20 mVpp30 mVpp sine @ 1kHz.

Also, check the fuse F1.

Table 6-6 defines the attenuator control line used in the high voltage output circuit. The relays in parenthesis are energized; all other relays are de-energized.

### 6.8.15 Frequency Synthesizer and Phase Lock Loop

This procedure steps you through the frequency synthesizer and phase lock loop. Also, refer to paragraph 5.4.4. Refer to the following drawings:

Motherboard assembly drawing 1101-00-3395.
Motherboard schematic 1104-00-3395 sheet 4.
Phase Lock Loop assembly drawing 1101-00-3341
Phase Lock Loop schematic 1104-00-3341 sheets 2 and 3.

Reset the unit by pressing SHIFT and RESET ALL keys.

1. Check the following test points on the frequency synthesizer (schematic 1104-00-3395 sheet 4). If the value at a test point is incorrect, isolate and repair the fault of the circuit between the good and bad test points.

**Table 6-6. HV Out Attenuator Control Lines**

| Voltage Output | Atten. | 20DBEN | 40DBEN | 60DBEN | LOAMPL |
|---|---|---|---|---|---|
| 40 Vpp to 4Vpp | 0dB | Low | Low | Low | High (K2) |
| 3.99 Vpp to 0.4 Vpp | 20 dB | High (K1) | Low | Low | High (K2) |
| 0.399 Vpp to 0.04 Vpp | 0/40 dB | Low | High (K3) | Low | Low |
| 39.9 mVpp to 4mVpp | 0/60 dB | Low | Low | High (K4) | Low |
| 3.999 mVpp to 1mVpp | 20/60 dB | High (K1) | Low | High (K4) | Low |
| Output Off. | | High | Low | Low | Low |

| | | |
|---|---|---|
| 18 | OSCIN | 3.5 Vpp square @ 500 kHz. |
| TP5 | VC LOOP | +3 Vdc Locked, and +5 Vdc Unlocked. |
| TP17 | SYOUT | 4Vp TTL 50 ns pulses @ 1kHz. |

2. Check the following test points on the phase lock loop (schematic 1104-00-3341 sheets 2, 3, and 4). If the value at a test point is incorrect, isolate and repair the fault of the circuit between the good and bad test points.

| | | |
|---|---|---|
| TP3 | SYNTH | ~4Vp TTL 50 ns pulses @ 1kHz. |
| TP1 | Z-CROSS | ~5Vpp Square @ 1kHz. |
| 19 | SQWAVE | ~3 Vpp Square @ 1kHz |
| 20 | 1Y | ~4Vp pulses |
| 21 | 2Y | ~3 Vpp square |
| 22 | | 3.5 Vp pulses |
| 23 | | 3.5 Vp pulses |
| TP7 | VLEADR | ~4Vp pulses @ 500 Hz. |
| TP8 | VLAGR | ~4Vp pulses @ 500 Hz. |
| TP9 | PLLER (VLOOP) | Locked: +0.1Vdc Unlocked: -12 Vdc. |

3 If Option 001 - Frequency Reference is installed, check the following test points on the phase lock loop (schematic 1104-00-3341 sheet 6).

| | | |
|---|---|---|
| TP11 | TCXO Output | ~4Vpp square @ 10 MHz ±1ppm. |
| TP12 | OSCIN | ~3.5 Vpp square @ 500 kHz. |
| REF OUT | TTL square @ 10 MHz. | |

Connect a 10 MHz TTL signal to the Ref In connector.

| | | |
|---|---|---|
| TP10 | EXTREF | TTL square @ 10 MHz. |

### 6.8.16 Microprocessor Section

1. Check the Microprocessor Section: Schematic 1104-00-3395 Sheet 3 of 10, Assembly drawing 1101-00-3395 sheet 1 of 3. For a description of the Microprocessor Section' circuits, refer to paragraph 5.6.2.
2. Observe the Microprocessor's Life Lite. During normal operation the Microprocessor's Life Lite blinks at a rate of about 2 or 3 blinks per second. If the Life Lite blinks, the Microprocessor Section is functioning correctly.

   Non-Blinking Life Lite - Microprocessor Section inoperative. The LED may be continuously on or off. If continuously on, the power supplies are probably operational and the fault is in the microprocessor circuits. If continuously off, the possibility of power supply failure should be checked prior to microprocessor circuit troubleshooting.
3. Check the supply voltages to the circuits within the Microprocessor Section.
4. Using the scope, check the control and data lines. Most lines should be "moving". Lines stuck high or low could identify a defective device.

### 6.8.17 DAC Sample and Hold Network

Refer to the Motherboard assembly drawing (1101-00-3395) and schematic (1104-00-3395 sheet 5) in section 7 of this manual. Also refer to the circuit description, paragraph 5.6.5 of this manual. Reset the unit by pressing SHIFT and RESET ALL keys.

Check the following test points. If the value at a test point is incorrect, isolate and repair the fault of the circuit between the good and bad test points.

| | | |
|---|---|---|
| TP7 | SHDAC | Verify a stepped waveform. |
| R33/R34 | VOFST | ~0Vdc |
| U21B-7 | VAMCAL | Verify a dc voltage. |
| U22B-7 | VSLEN | Verify a dc voltage. |
| U23B-7 | VFREQ | Verify a dc voltage. |
| U22A-1 | VCGZERO | Verify a dc voltage. |
| U24B-7 | VPHASE | Verify a dc voltage. |
| U21A-1 | VSINCAL | Verify a dc voltage. |
| U24A-1 | VTRIBAL | Verify a dc voltage. |

### 6.8.18 GPIB Section

Refer to the Motherboard assembly drawing (1101-00-3395) and schematic (1104-00-3395 sheet 10) in section 7 of this manual. Also refer to the circuit description, paragraph 5.6.3 of this manual.

To troubleshoot the GPIB section,

1. Check the digital control lines to the GPIB board. Verify the overhead signals work correctly (E clock, Read/Write, chip select).
2. Check the address and data lines between the GPIA (U8) and the microprocessor section.
3. Check the lines connecting the GPIA and transceiver (U9 and U10).
4. Check the lines between the transceiver and the GPIB controller.

### 6.8.19 Board Interfaces

Each of the Model 90 boards contain interface circuits that "translates" address/data information from the microprocessor section for use on the board. Troubleshooting these interfaces by checking the each board's

enable lines and verifying the activity on the address and data lines.

Function Generator Board Interface
Schematic: 1104-00-3342 sheet 1.
Assembly: 1101-00-3342
Circuit Description: paragraph 5.6.4.1.

Phase Lock Loop Board Interface
Schematic: 1104-00-3341 sheet 1.
Assembly: 1101-00-3341
Circuit Description: paragraph 5.6.4.2.

Aux Board Interface
Schematic: 1104-00-3386 sheet 1.
Assembly: 1101-00-3386
Circuit Description: paragraph 5.6.4.3.

Output Board Interface
Schematic: 1104-00-3335 sheet 1.
Assembly: 1101-00-3335
Circuit Description: paragraph 5.6.4.4.

Front Panel Interface
Schematic: 1104-00-3322 sheet 2.
Assembly: 1101-00-3322
Circuit Description: paragraph 5.6.4.5.

## 6.9 Disassembly and Reassembly

### 6.9.1 Disassembly

#### Top Cover/Shield Removal

To remove the top cover and shield,

1. Set the POWER switch to OFF (extended).
2. Remove the power cable from the rear panel power connector.
3. Remove the five screws that secure the top cover; four in the top and one at the rear.
   Two of the four top cover screws are located under the Calibration Label.
4. Slide the top cover toward the rear and remove. Then lift off the shield.

#### Bottom Cover Removal

To remove the bottom cover,

1. Set the POWER switch to OFF (extended).
2. Remove the power cable from the rear panel power connector.
3. Remove the three screws that secure the bottom cover; one in the bottom cover and two in the rear. The one screw on the bottom cover is located under the Calibration Label.
4. Slide the bottom cover towards the rear and remove.

### 6.9.2 Board Removal/Replacement

To remove the Output, PLL, Function Generator, or Aux board,

1. Perform the steps in paragraph 6.9.1 - Top Cover/ Shield Removal.
2. Disconnect the cable from the Output Board. Disconnect the four cables from the Aux Board.
3. Lift out the board using the extractors.

To replace the Output, PLL, Function Generator, or Aux board

1. Place the board in its guide and press it down to lock it in the connector
2. Connect the cable to the Output Board. Connect the four cables to the Aux Board.
3 Perform the steps in paragraph 6.9.3 - Top Cover/ Shield Reassembly.

### 6.9.3 Reassembly

#### Bottom Cover Replacement

To replace the bottom cover,

1. Turn the Model 90 upside down.
2. Slide the bottom cover into the slots on the bottom.
3. Secure the bottom cover with three screws (two in the rear and one on the bottom cover).

#### Top Cover Replacement

Top replace the top cover,

1. Turn the Model right side up.
2. Install the shield, aligning the screw holes.
3. Slide the top cover into the slots on the top.
4. Secure the top cover using five screws (one at the rear and four in the top). The four top cover screws must line up with the holes in the shield.

### 7.1 Drawings

The following assembly drawings, schematics, and parts lists are arranged in order shown below.

#### 7.1.1 Assembly Drawing

All of the mechanical assembly drawings are show in this section. These drawings contain enough detail and clarity to assist the repair technician in the disassembly and reassembly of the Model 90 The parts lists for each assembly drawing immediately follow that drawing.

#### 7.1.2. Schematics

All of the schematics for the Model 90 are shown in this section. Schematic drawings containing a proprietary message may not be copied for resale or use in any other publication nor for any use other than the repair and maintenance of the instrument associated with this manual.

#### 7.1.3 Parts Lists

The parts lists for each individual board or assembly are shown immediately following that board or assembly. The parts lists contain Wavetek and manufacturers parts information. All manufacturers are listed by a Wavetek code designation.

### 7.2 Addenda

Under Wavetek's product improvement program, the latest electronic designs and circuits are incorporated into each Wavetek instrument as quickly as development and testing permits. Because of the time needed to compose and print instruction manuals, it is not always possible to include the most recent changes in the initial printing. Whenever this occurs, addendum pages are prepared to summarize the changes made and are inserted immediately inside the rear cover. If no such pages exist, the manual is correct as printed.

### 7.3 Ordering Parts

When ordering spare parts, please specify the part number, circuit reference, board, serial number of the unit, and, if applicable, the function performed.

The number etched into a PC board is the board part number. The assembly (PC board and components on the board) part number is stamped on the board.

| DRAWING | NUMBER |
|---|---|
| Top Assembly Drawing | 1001-00-0596 |
| Instrument Schematic | 1004-00-0596 |
| Instrument Parts List | 1000-00-0606 |
| Installation Drawing | 0002-00-0596 |
| | |
| Motherboard Schematic | 1104-00-3395 |
| Motherboard Assembly | 1101-00-3395 |
| Motherboard Parts List | 1100-00-3395 |
| Motherboard Prewave Parts List | 1200-00-3390 |
| Front Panel Assembly | 1101-00-3321 |

| DRAWING | DRAWING NUMBER |
|---|---|
| Front Panel Assembly Parts List | 1100-00-3321 |
| Display/Keyboard Assembly Schematic | 1104-00-3322 |
| Display /Keyboard Assembly | 1101-00-3322 |
| Display /Keyboard Assembly Parts List | 1100-00-3322 |
| | |
| Output Board Schematic | 1104-00-3335 |
| Output Board Assembly | 1101-00-3335 |
| Output Board Parts List | 1100-00-3335 |
| | |
| Phase Lock Board Schematic | 1104-00-3437 |
| Phase Lock Board Assembly | 1101-00-3437 |
| Phase Lock Board Parts List | 1100-00-3437 |
| | |
| Function Generator Board Schematic | 1104-00-3342 |
| Function Generator Board Assembly | 1101-00-3342 |
| Function Generator Board Parts List | 1100-00-3342 |
| | |
| Auxiliary Board Schematic | 1104-00-3386 |
| Auxiliary Board Assembly | 1101-00-3386 |
| Auxiliary Board Parts List | 1100-00-3389 |
| | |
| Rear Panel Assembly | 1101-00-3325 |
| Rear Panel Assembly Parts List | 1100-00-3325 |
| | |
| Tilt Bail Assembly | 1201-00-3392 |
| Tilt Bail Parts List | 1200-00-3392 |

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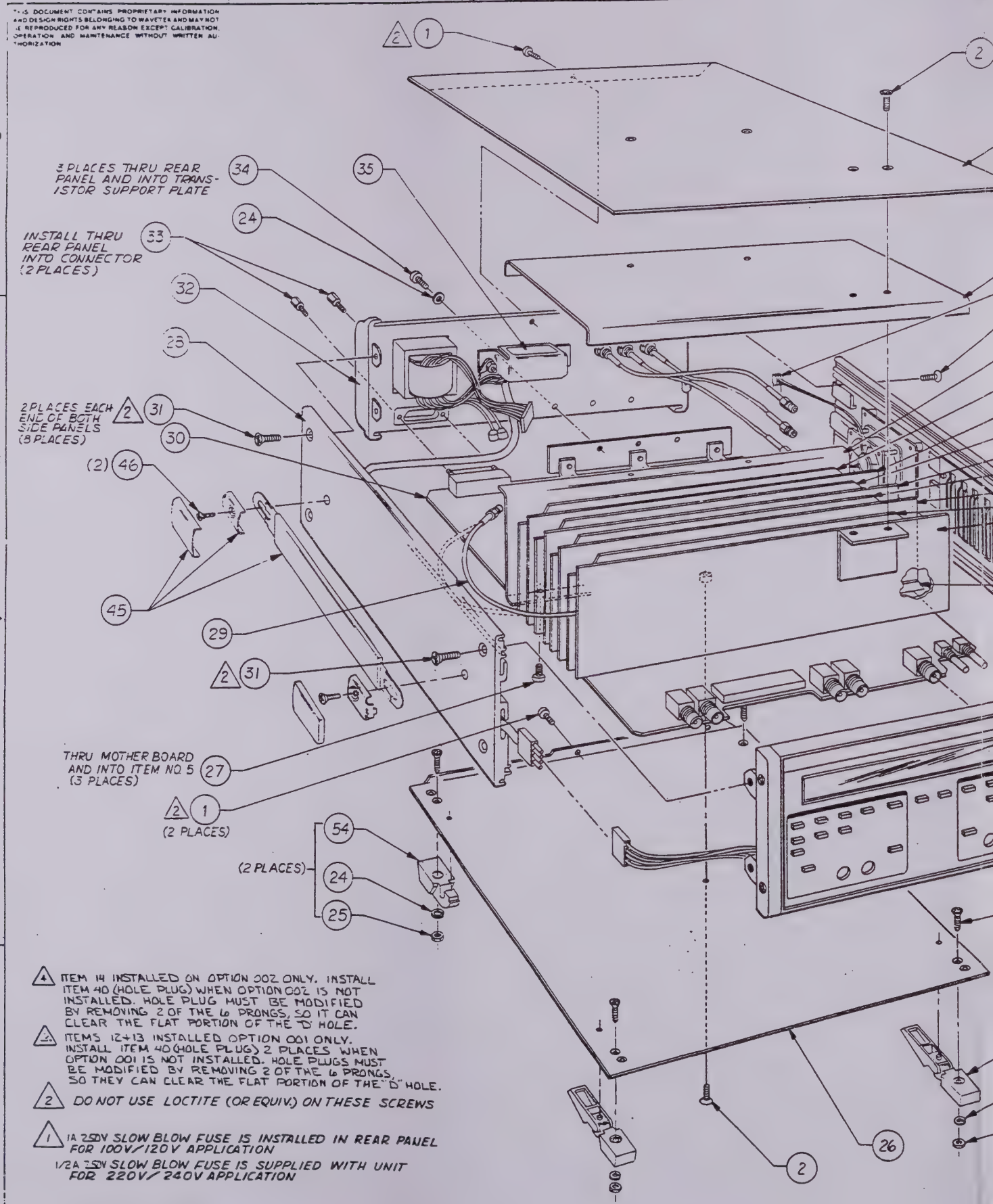

3 PLACES THRU REAR PANEL AND INTO TRANSISTOR SUPPORT PLATE
INSTALL THRU REAR PANEL INTO CONNECTOR (2 PLACES)
2 PLACES EACH END OF BOTH SIDE PANELS (8 PLACES)
(2)
THRU MOTHER BOARD AND INTO ITEM NO 5 (5 PLACES)
(2 PLACES)
(2 PLACES)
26

4 ITEM 14 INSTALLED ON OPTION 002 ONLY. INSTALL ITEM 40 (HOLE PLUG) WHEN OPTION 002 IS NOT INSTALLED. HOLE PLUG MUST BE MODIFIED BY REMOVING 2 OF THE 6 PRONGS, SO IT CAN CLEAR THE FLAT PORTION OF THE "D" HOLE.

3 ITEMS 12+13 INSTALLED OPTION 001 ONLY. INSTALL ITEM 40 (HOLE PLUG) 2 PLACES WHEN OPTION 001 IS NOT INSTALLED. HOLE PLUGS MUST BE MODIFIED BY REMOVING 2 OF THE 6 PRONGS, SO THEY CAN CLEAR THE FLAT PORTION OF THE "D" HOLE.

2 DO NOT USE LOCTITE (OR EQUIV.) ON THESE SCREWS

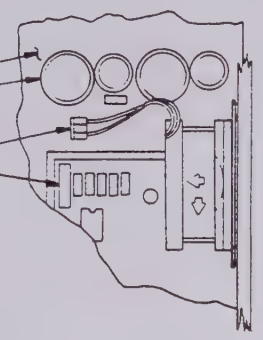
1 1A 250V SLOW BLOW FUSE IS INSTALLED IN REAR PANEL FOR 100V/120V APPLICATION
1/2A 250V SLOW BLOW FUSE IS SUPPLIED WITH UNIT FOR 220V/240V APPLICATION

NOTE UNLESS OTHERWISE SPECIFIED

| REV | ECO | BY | DATE | APP |
|---|---|---|---|---|
| A | ERO NO. 91-116 | AD | [illegible] | [illegible] |
| B | ECO # 90-521 | MS | [illegible] | [illegible] |
| C | ECO # 90 5660 | MS | [illegible] | [illegible] |
| D | ECO # 91-009 | [illegible] | [illegible] | [illegible] |
| E | ECO # 91-106 | [illegible] | [illegible] | [illegible] |
| F | ECO NO 91-403 | [illegible] | [illegible] | [illegible] |

PLACES)

3




VIEW "A"
POWER CONNECTOR, FAN

4

SEE VIEW "A"

31 2

5 SEE VIEW "B" FOR LABEL INSTALLATION ONTO ITEM NO. 5

6

7

8

7

9

7

10

11

31 2

REF. HEMMED EDGE IS LOCATED TOWARD FRONT ON ITEM NO. 7 (3 PLACES)

12 3

13 3

14 4

15

16

19

1 18

17

42 INSTALL LABEL IN APPROXIMATE LOCATION SHOWN

20 (5 PLACES)

22 (4 PLACES)

5 REF

VIEW "B"
VIEWED FROM REAR OF INSTRUMENT

53

24 (2 PLACES)

25

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL

FINISH
WAVETEK PROCESS

DO NOT SCALE DRAWING

| | | |
|---|---|---|
| DRAWN | D. COOPER | 5-11-90 |
| CHECKED | | 6/26/90 |
| ENGINEER | | 6/26/90 |
| RELEASE APPROV. | | 6/29/90 |

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
± / XX ± / ±
XXX ± /

WAVETEK SAN DIEGO, CALIFORNIA

TITLE
TOP ASSEMBLY DRAWING

| SIZE | FSCM NO. | DWG. NO. | REV |
|---|---|---|---|
| D | 23338 | 1001-00-0596 | F |

SCALE NONE | MODEL 90 | SHEET 1 OF 1

1001-00-0596 F

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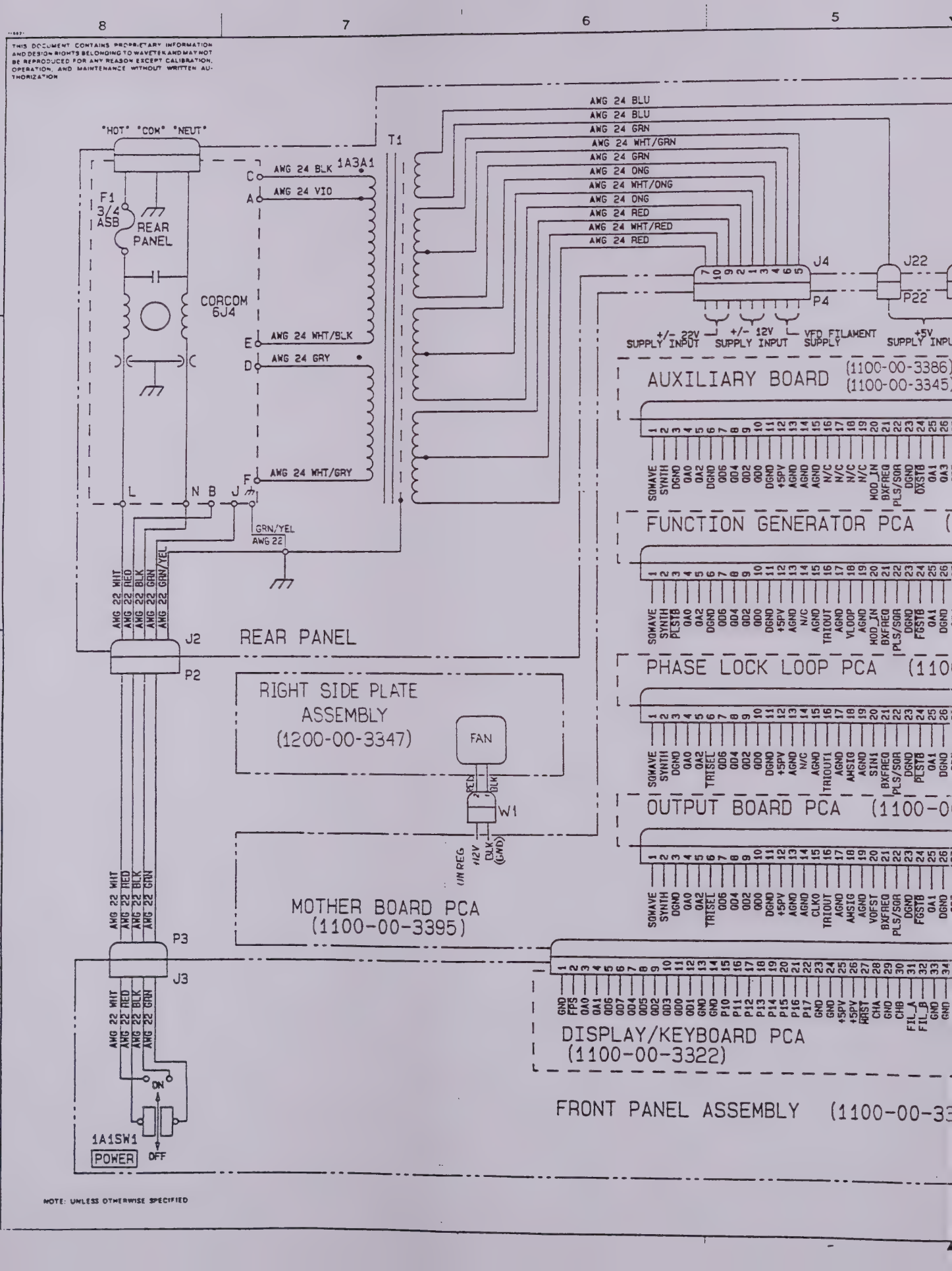
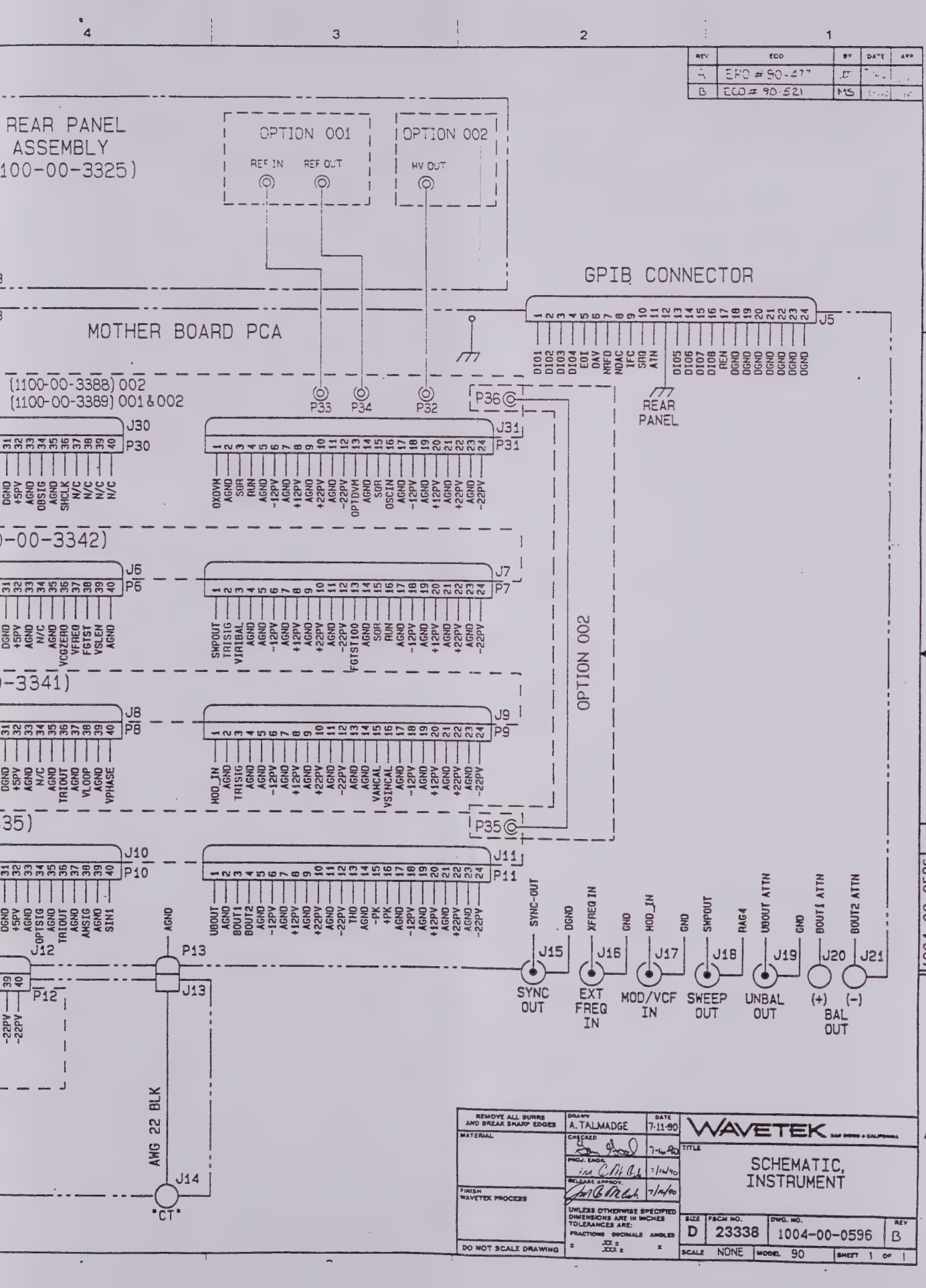



NOTE: UNLESS OTHERWISE SPECIFIED


REV
ECO
BY
DATE
APP
A
ECO # 90-477
B
ECO # 90-521
MS
REAR PANEL ASSEMBLY
(100-00-3325)
OPTION 001
REF IN
REF OUT
OPTION 002
HV OUT
GPIB CONNECTOR
J5
DIO1
DIO2
DIO3
DIO4
EOI
DAV
NRFD
NDAC
IFC
SRQ
ATN
DIO5
DIO6
DIO7
DIO8
REN
DGND
MOTHER BOARD PCA
(1100-00-3388) 002
(1100-00-3389) 001&002
P33
P34
P32
P36
REAR PANEL
J30
P30
J31
P31
DGND
+5PV
AGND
OBSIG
AGND
SHCLK
N/C
OXDVM
SOR
RUN
-12PV
+12PV
+22PV
-22PV
OPTDVM
OSCIN
-00-3342)
J6
P6
J7
P7
VCGZERO
VFREQ
FGTST
VSLEN
SWPOUT
TRISIG
VIRTBAL
FGTST100
-3341)
J8
P8
J9
P9
TRIOUT
VLOOP
VPHASE
MOD_IN
VAMCAL
VSINCAL
OPTION 002
35)
P35
J10
P10
J11
P11
OPTSIG
AMSIG
SIN1
UBOUT
BOUT1
BOUT2
THO
-PK
+PK
J12
P12
P13
J13
J14
AWG 22 BLK
"CT"
SYNC-OUT
XFREQ IN
MOD_IN
SWPOUT
RAG4
UBOUT ATTN
BOUT1 ATTN
BOUT2 ATTN
J15
J16
J17
J18
J19
J20
J21
SYNC OUT
EXT FREQ IN
MOD/VCF IN
SWEEP OUT
UNBAL OUT
(+)
(-)
BAL OUT
1004-00-0596
B
REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DO NOT SCALE DRAWING
DRAWN
A. TALMADGE
7-11-90
CHECKED
PROJ. ENGR.
RELEASE APPROV.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
WAVETEK
TITLE
SCHEMATIC, INSTRUMENT
SIZE
D
FSCM NO.
23338
DWG. NO.
1004-00-0596
REV
B
SCALE
NONE
MODEL
90
SHEET 1 OF 1

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| REFERENCE DESIGNATORS | PART DESCRIPTION |
|---|---|
| 15 | LABEL, SMB CONNECTOR |
| 5 | SHIELD, REAR |
| 42 | LABEL, CABLE ORIENTATION |
| 33 | HARDWARE KIT, GPIB CONN |
| 18 | FUSE, 1A, 250V, S-B |
| 45 | HANDLE, RETRACTABLE |
| 54 | FOOT |
| 53 | FOOT WITH TIP-UP |
| 20 | NUT, HEX, 1/2-28 |
| 25 | NUT, HEX, 8-32, 3/32 THK, 25 FLT, MINI, SS |
| 24 | LOCKWASHER, #8 SPLIT RING, SS |
| 1 | SCREW PLPS PAN M/S 18-8 S/S 6-32X3/8 |
| 34 | SCREW PLPS PAN M/S 18-8 S/S 8-32X1/2 |
| 31 | SCREW, 8-32X7/16, 100DE |

WAVETEK PARTS LIST

TITLE
MODEL 90 W/001/002 H.V. AN TCXO REFERENCE

| REFERENCE DESIGNATORS | PART DESCRIPTION |
|---|---|
| | C FH, PHLPS, SS |
| 22 | SCREW, 8-32 X 1/2, 100 DEG, FH, PHLPS, SS |
| 27 | SCREW, PH, 6-32 X 5/16, PHLPS, NYLOK, SS |
| 2 | SCREW, 6-32/3/8, FH, PHL PS, 100DEG, SS, NYLOK, PA TCH |
| NONE | PWR CORD, SHIELDED |

WAVETEK PARTS LIST

TITLE
MODEL 90 W/001/002 H.V. AN TCXO REFERENCE

NOTE UNLESS OTHERWISE SPECIFIED

8 7 6 5

D C B A

| REV | ECO | BY | DATE | APP |
|---|---|---|---|---|

| MFGR-PART-NO | MFGR | WAVETEK NO | QTY/PT |
|---|---|---|---|
| 02-5070 | WVTK | 1400-02-5070 | 1 |
| 02-5084 | WVTK | 1400-02-5084 | 1 |
| 02-5117 | WVTK | 1400-02-5117 | 1 |
| B-1 | AMP | 2100-07-0024 | 1 |
| | BUSS | 2400-05-0029 | 1 |
| 07-0035 | WAVTK | 2800-07-0035 | 1 |
| -026 | SCHRF | 2800-08-0020 | 2 |
| -025 | SCHRF | 2800-08-0021 | 2 |
| 631-2 | AMP | 2800-16-0025 | 5 |
| 16-8106 | CMCRL | 2800-16-8106 | 4 |
| W | CMRCL | 2800-42-8000 | 7 |
| 957-28 | CMRCL | 2800-48-6106 | 3 |
| PH B-32X1/2 | CMRCL | 2800-48-8108 | 3 |
| 54-8107 | CMCRL | 2800-54-8107 | 8 |

| | ASSEMBLY NO. 1000-00-0606 | REV M |
|---|---|---|
| | PAGE 3 | |

| REFERENCE DESIGNATORS | PART DESCRIPTION | ORIG-MFGR-PART-NO | MFGR | WAVETEK NO | QTY/PT |
|---|---|---|---|---|---|
| 46 | SCREW, 6-32 X 1/2, FH, ZINC, 100 DEG | 0203-00014 | VIC-T | 0203-00014 | 2 |
| NONE | TOP ASSY DRAWING, MODEL 90 | 1001-00-0596 | WVTK | 1001-00-0596 | 1 |
| NONE | ACCEPTANCE TEST SPECIFICATION MODEL 90 | 1002-00-0596 | WVTK | 1002-00-0596 | 1 |
| NONE | BLOCK DIAGRAM, MODEL 90 | 1003-00-0596 | WVTK | 1003-00-0596 | 1 |
| NONE | INSTRUMENT SCHEMATIC, MODEL 90 | 1004-00-0596 | WVTK | 1004-00-0596 | 1 |
| REF | MODEL 90 INSTRUCTION MANUAL | 1006-00-0596 | WVTK | 1006-00-0596 | 1 |
| NONE | MODEL 90 MAINTENANCE MANUAL | 1006-00-0596-2 | WVTK | 1006-00-0596-2 | 1 |
| NONE | CALIBRATION PROCEDURE, MODEL 90 | 1008-00-0596 | WVTK | 1008-00-0596 | 1 |
| 16 | LABEL/DRWG. INFO. S/N & PWR-90 | 1009-00-0596 | WVTK | 1009-00-0596 | 1 |
| 19 | FRONT PANEL ASSY MODEL 90 | 1100-00-3321-01 | WVTK | 1100-00-3321-01 | 1 |
| 10 | PCA, OUTPUT BOARD | 1100-00-3335 | WVTK | 1100-00-3335 | 1 |

| WAVETEK PARTS LIST | TITLE MODEL 90 W/001/002 H.V. AND TCXO REFERENCE | ASSEMBLY NO. 1000-00-0606 | REV M |
|---|---|---|---|
| | | PAGE 1 | |

| MFGR-PART-NO | MFGR | WAVETEK NO. | QTY/PT |
|---|---|---|---|
| 54-8108 | CMCRL | 2800-54-8108 | 4 |
| 59-6105 | CMRCL | 2800-59-6105 | 3 |
| 60-6106 | CMRCL | 2800-60-6106 | 3 |
| 80-0009 | WVTK | 6001-80-0009 | 1 |

| | ASSEMBLY NO. 1000-00-0606 | REV M |
|---|---|---|
| | PAGE 4 | |

| REFERENCE DESIGNATORS | PART DESCRIPTION | ORIG-MFGR-PART-NO | MFGR | WAVETEK NO. | QTY/PT |
|---|---|---|---|---|---|
| 8 | PCA, FUNCTION GENERATOR | 1100-00-3342 | WVTK | 1100-00-3342 | 1 |
| 6 | PCA, AUX BD, OPT 001&002 | 1100-00-3389 | WVTK | 1100-00-3389 | 1 |
| 9 | PCA, PHASE LOCK LOOP | 1100-00-3437 | WVTK | 1100-00-3437 | 1 |
| 32A | REAR PANEL ASSY 90/95 | 1100-00-3583 | WVTK | 1100-00-3583 | 1 |
| 30 | PCA MOTHER BD MODEL 90 | 1100-00-3607-02 | WVTK | 1100-00-3607-02 | 1 |
| 29 | ASSEMBLY, COAX AUX BOARD | 1200-00-3400 | WVTK | 1200-00-3400 | 1 |
| 11 | SIDE PANEL ASSY, RIGHT | 1200-00-3582 | WVTK | 1200-00-3582 | 1 |
| 28 | LEFT SIDE PANEL | 1200-00-3593 | WVTK | 1200-00-3593 | 1 |
| 35 | LABEL, CAUTION | 859-1400 | WVTK | 1400-01-1400 | 1 |
| 17 | LABEL, OPTION, MODEL 23 | 1400-01-9890 | WVTK | 1400-01-9890 | 1 |
| 7 | SHIELD, INNER | 1400-02-3323 | WVTK | 1400-02-3323 | 3 |
| 4 | SHIELD, TOP | 1400-02-3353 | WVTK | 1400-02-3353 | 1 |
| 3 | COVER, TOP | 1400-02-3532 | WVTK | 1400-02-3532 | 1 |
| 26 | COVER, BOTTOM | 1400-02-4322 | WVTK | 1400-02-4322 | 1 |

| WAVETEK PARTS LIST | TITLE MODEL 90 W/001/002 H.V. AND TCXO REFERENCE | ASSEMBLY NO. 1000-00-0606 | REV M |
|---|---|---|---|
| | | PAGE 2 | |

| | | | |
|---|---|---|---|
| REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN | DATE | WAVETEK SAN DIEGO, CALIFORNIA |
| MATERIAL | CHECKED | | TITLE PARTS LIST INSTRUMENT |
| | PROJ. ENGR | | |
| | RELEASE APPROV. | | |
| FINISH WAVETEK PROCESS | UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ± .XXX ± | | SIZE D FSCM NO. 23338 DWG. NO. 1000-00-0606 REV M |
| DO NOT SCALE DRAWING | | | SCALE MODEL 90 SHEET 1 OF 1 |

4 3 2 1

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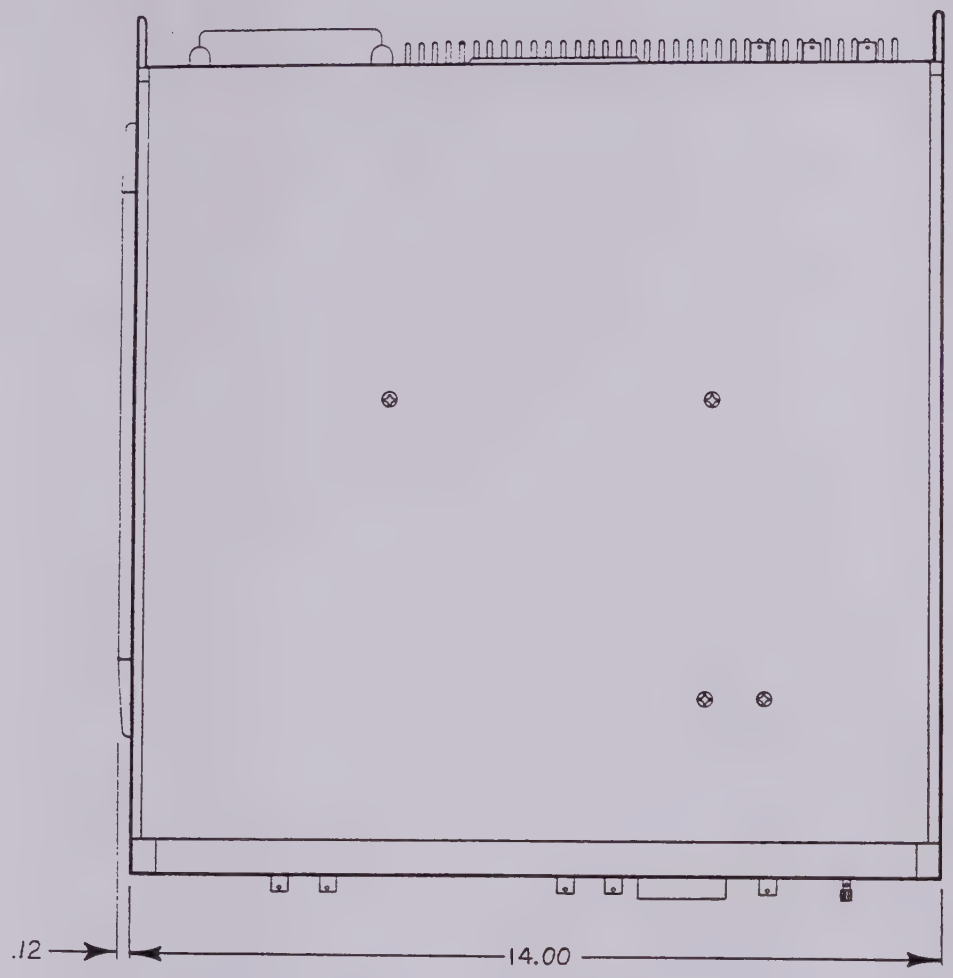
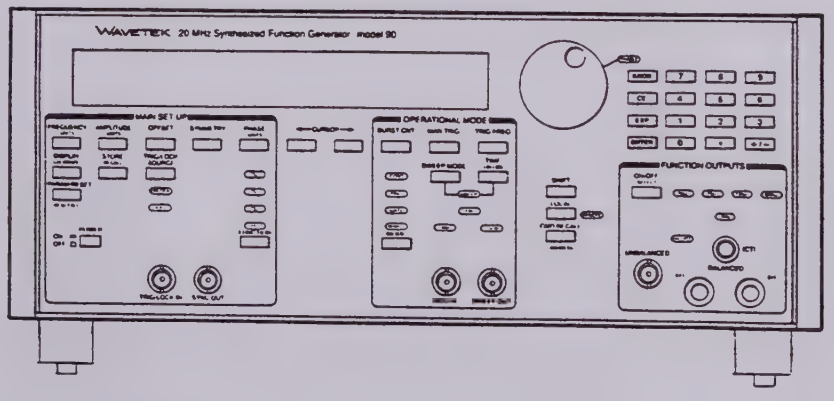
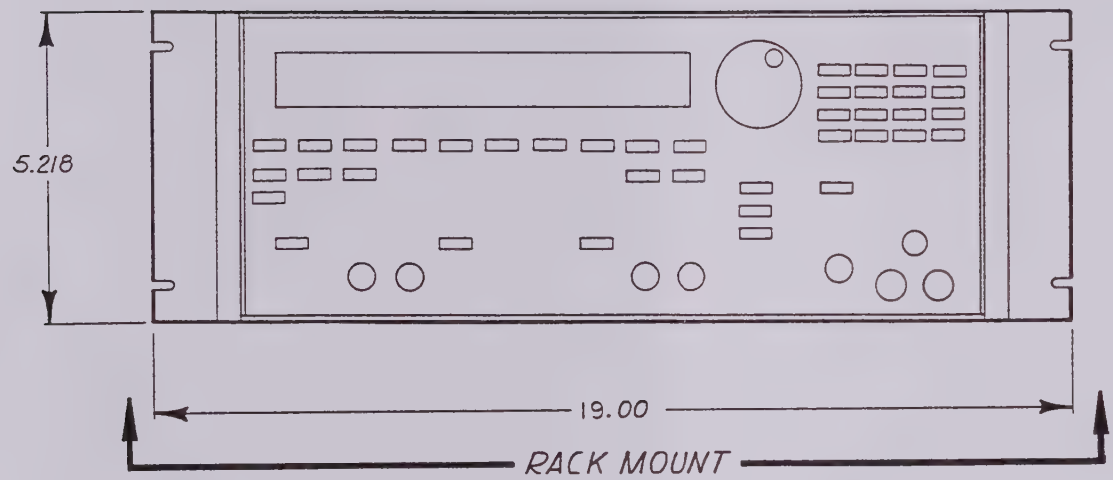
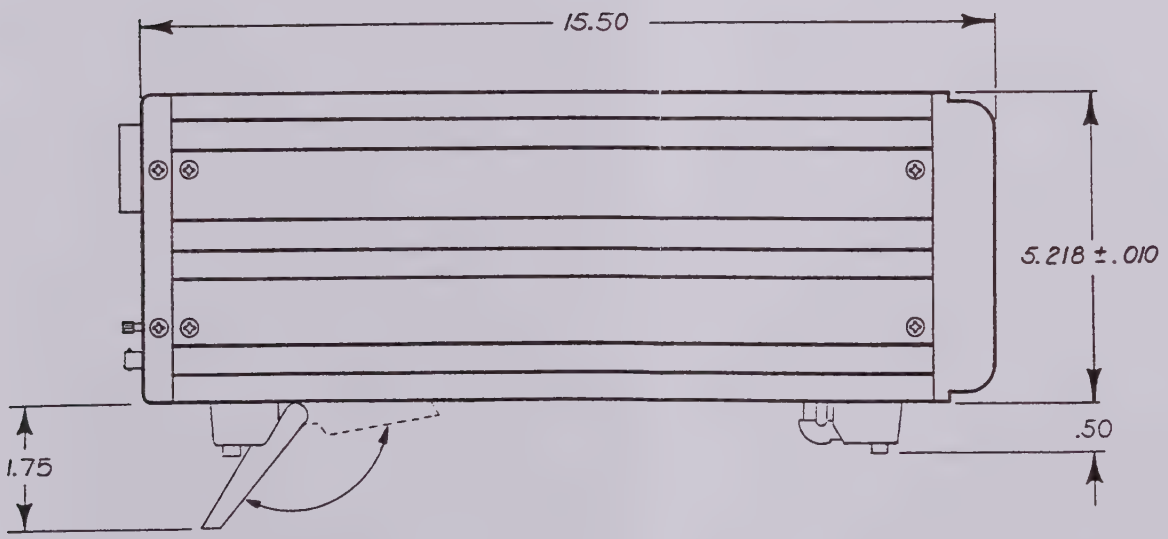



NOTE UNLESS OTHERWISE SPECIFIED

| REV | ECO | BY | DATE | APP |
|---|---|---|---|---|
| A | ERO. NO. [illegible] | AP | [illegible] | [illegible] |
| B | ECO # 91-267 | RA | 5/16/91 | |
| C | ECO # [illegible] | [illegible] | [illegible] | [illegible] |




| | | | |
|---|---|---|---|
| REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN: D. COOPER | DATE: 5-11-90 | WAVETEK SAN DIEGO, CALIFORNIA |
| MATERIAL | CHECKED: [signature] | [illegible] | TITLE: INSTALLATION DRAWING |
| FINISH WAVETEK PROCESS | PROD. ENGR.: [signature] | [illegible] | |
| DO NOT SCALE DRAWING | RELEASE APPROV.: [signature] | [illegible] | SIZE: D; FSCM NO.: 23338; DWG. NO.: 0002-00-0596; REV: C |
| UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ± / XX ± .03 XXX ± .010 ± 1° | | | SCALE: 3/4; MODEL: 90; SHEET 1 OF 1 |

0002-00-0596 C

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## FRONT PANEL BOARD CONNECTOR

J12

| | |
|---|---|
| DGND | 1 |
| QA0 | 2 |
| QD6 | 3 |
| QD4 | 4 |
| QD2 | 5 |
| QD0 | 6 |
| DGND | 7 |
| P10 | 8 |
| P12 | 9 |
| P14 | 10 |
| P16 | 11 |
| DGND | 12 |
| +5PV | 13 |
| DGND | 14 |
| DGND | 15 |
| FIL_A | 16 |
| DGND | 17 |
| +24PV | 18 |
| DGND | 19 |
| -24PV | 20 |
| $\overline{\text{FPSTB}}$ | 21 |
| QA1 | 22 |
| QD7 | 23 |
| QD5 | 24 |
| QD3 | 25 |
| QD1 | 26 |
| DGND | 27 |
| P11 | 28 |
| P13 | 29 |
| P15 | 30 |
| P17 | 31 |
| DGND | 32 |
| +5PV | 33 |
| RKA | 34 |
| RKB | 35 |
| FIL_B | 36 |
| DGND | 37 |
| +24PV | 38 |
| DGND | 39 |
| -24PV | 40 |

## OUTPUT BOARD CONNECTORS

P10

| | |
|---|---|
| SQWAVE | 1 |
| SYNTH | 2 |
| DGND | 3 |
| QA0 | 4 |
| QA2 | 5 |
| $\overline{\text{TRISEL}}$ | 6 |
| QD6 | 7 |
| QD4 | 8 |
| QD2 | 9 |
| QD0 | 10 |
| DGND | 11 |
| +5PV | 12 |
| AGND | 13 |
| | 14 |
| CLK0 | 15 |
| TRIOUT1 | 16 |
| AGND | 17 |
| AMSIG | 18 |
| AGND | 19 |
| VOFST | 20 |
| BXFREQ | 21 |
| PLS/SQR | 22 |
| DGND | 23 |
| $\overline{\text{OBSTB}}$ | 24 |
| QA1 | 25 |
| DGND | 26 |
| QD7 | 27 |
| QD5 | 28 |
| QD3 | 29 |
| QD1 | 30 |
| DGND | 31 |
| +5PV | 32 |
| AGND | 33 |
| OBSIG | 34 |
| AGND | 35 |
| | 36 |
| AGND | 37 |
| AMSIG | 38 |
| AGND | 39 |
| SIN1 | 40 |

P11

| | |
|---|---|
| UBOUT | 1 |
| AGND | 2 |
| BOUT1 | 3 |
| BOUT2 | 4 |
| AGND | 5 |
| -12PV | 6 |
| AGND | 7 |
| +12PV | 8 |
| AGND | 9 |
| +24PV | 10 |
| AGND | 11 |
| -24PV | 12 |
| THD | 13 |
| AGND | 14 |
| -PK | 15 |
| +PK | 16 |
| AGND | 17 |
| -12PV | 18 |
| AGND | 19 |
| +12PV | 20 |
| AGND | 21 |
| +24PV | 22 |
| AGND | 23 |
| -24PV | 24 |

## PHASE L BOARD C

| | |
|---|---|
| SQWAVE | |
| SYNTH | |
| DGND | |
| QA0 | |
| QA2 | |
| $\overline{\text{TRISEL}}$ | |
| QD6 | |
| QD4 | |
| QD2 | |
| QD0 | |
| DGND | |
| +5PV | |
| AGND | |
| | |
| TRIOUT1 | |
| AGND | |
| AMSIG | |
| AGND | |
| SIN1 | |
| BXFREQ | |
| PLS/SQR | |
| DGND | |
| $\overline{\text{PLSTB}}$ | |
| QA1 | |
| DGND | |
| QD7 | |
| QD5 | |
| QD3 | |
| QD1 | |
| DGND | |
| +5PV | |
| AGND | |
| | |
| AGND | |
| VLOOP | |
| AGND | |
| VPHASE | |

| | |
|---|---|
| MOD_IN | |
| AGND | |
| TRISIG | |
| AGND | |
| | |
| -12PV | |
| AGND | |
| +12PV | |
| AGND | |
| +24PV | |
| AGND | |
| -24PV | |
| AGND | |
| | |
| VAMCAL | |
| VSINCAL | |
| AGND | |
| -12PV | |
| AGND | |
| +12PV | |
| AGND | |
| +24PV | |
| AGND | |
| -24PV | |

## POWER SUPPLY UNREGULATED AC INPUT

P4

| | |
|---|---|
| 1, 2, 3 | +/-12V SUPPLY UNREGULATED VOLTAGE |
| 4, 5, 6 | VFD FILAMENT SUPPLY |
| 7, 8, 9, 10 | +/-24 SUPPLY UNREGULATED VOLTAGE |
| P23, P22 | +5V REGULATED SUPPLY |

9. TEST POINTS SHOWN AS ✡ ARE FAULT ISOLATION PROCEDURES IN THE UNIT MAINTENANCE MANUAL.
8. ⏚D =DGND. ⏚A =AGND.
7. SEE BILL OF MATERIALS FOR PROGRAMMED PART NUMBER.
6. * = PART INSTALLED IN SOCKET.
5. CAPACITORS VALUED IN MICROFRADS (uF).
4. RESISTORS VALUED IN OHMS, 1/8W, 5%.
3. FOR INSTRUMENT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 1004-00-0596 FOR MODEL 90 AND 1004-00-0599 FOR MODEL 95.
2. INSTALL JMP1 ON PINS 1 & 2 FOR BIPOLAR EXT FREQ INPUTS. INSTALL ON PINS 2 & 3 FOR TTL EXT FREQ INPUTS.
1. INSTALL JMP7 ON PINS 1 & 2 FOR STANDARD INSTRUMENT. INSTALL ON PINS 2 & 3 FOR OPTION 001.

NOTE UNLESS OTHERWISE SPECIFIED

| REV | ECO | BY | DATE | APP |
|---|---|---|---|---|
| A | ECO #: 90-462 | [illegible] | [illegible] | [illegible] |
| B | ECO #: 90-506 | MS | 5-14-90 | [illegible] |
| C | ECO #: 90-521 | MS | 10/15/90 | [illegible] |
| D | ECO #: 91-116 | [illegible] | [illegible] | |

## FUNCTION GENERATOR BOARD CONNECTORS

### P6

| | |
|---|---|
| SQWAVE | 1 |
| SYNTH | 2 |
| PLSTB | 3 |
| QA0 | 4 |
| QA2 | 5 |
| DGND | 6 |
| QD6 | 7 |
| QD4 | 8 |
| QD2 | 9 |
| QD0 | 10 |
| DGND | 11 |
| +5PV | 12 |
| AGND | 13 |
| | 14 |
| | 15 |
| | 16 |
| AGND | 17 |
| VLOOP | 18 |
| AGND | 19 |
| MOD_IN | 20 |
| BXFREQ | 21 |
| PLS/SQR | 22 |
| DGND | 23 |
| FGSTB | 24 |
| QA1 | 25 |
| DGND | 26 |
| QD7 | 27 |
| QD5 | 28 |
| QD3 | 29 |
| QD1 | 30 |
| DGND | 31 |
| +5PV | 32 |
| AGND | 33 |
| | 34 |
| | 35 |
| VCGZERO | 36 |
| VFREQ | 37 |
| FGTST | 38 |
| VSLEN | 39 |
| AGND | 40 |

### P7

| | |
|---|---|
| SWPOUT | 1 |
| TRISIG | 2 |
| VTRIBAL | 3 |
| AGND | 4 |
| | 5 |
| -12PV | 6 |
| AGND | 7 |
| +12PV | 8 |
| AGND | 9 |
| +24PV | 10 |
| AGND | 11 |
| -24PV | 12 |
| FGTST100 | 13 |
| AGND | 14 |
| SQR | 15 |
| RUN | 16 |
| AGND | 17 |
| -12PV | 18 |
| AGND | 19 |
| +12PV | 20 |
| AGND | 21 |
| +24PV | 22 |
| AGND | 23 |
| -24PV | 24 |

## AUXILLARY BOARD CONNECTORS

### P30

| | |
|---|---|
| SQWAVE | 1 |
| SYNTH | 2 |
| DGND | 3 |
| QA0 | 4 |
| QA2 | 5 |
| DGND | 6 |
| QD6 | 7 |
| QD4 | 8 |
| QD2 | 9 |
| QD0 | 10 |
| DGND | 11 |
| +5PV | 12 |
| AGND | 13 |
| | 14 |
| | 15 |
| | 16 |
| | 17 |
| | 18 |
| | 19 |
| MOD_IN | 20 |
| BXFREQ | 21 |
| PLS/SQR | 22 |
| DGND | 23 |
| OXSTB | 24 |
| QA1 | 25 |
| QA3 | 26 |
| QD7 | 27 |
| QD5 | 28 |
| QD3 | 29 |
| QD0 | 30 |
| DGND | 31 |
| +5PV | 32 |
| AGND | 33 |
| OBSIG | 34 |
| AGND | 35 |
| SHCLK | 36 |
| | 37 |
| | 38 |
| | 39 |
| POE | 40 |

### P31

| | |
|---|---|
| OPTDVM1 | 1 |
| AGND | 2 |
| SQR | 3 |
| RUN | 4 |
| AGND | 5 |
| -12PV | 6 |
| AGND | 7 |
| +12PV | 8 |
| AGND | 9 |
| +24PV | 10 |
| AGND | 11 |
| -24PV | 12 |
| OPTDVM2 | 13 |
| AGND | 14 |
| | 15 |
| OSCIN | 16 |
| AGND | 17 |
| -12PV | 18 |
| AGND | 19 |
| +12PV | 20 |
| AGND | 21 |
| +24PV | 22 |
| AGND | 23 |
| -24PV | 24 |

CAD JOB#: B064E

| | | |
|---|---|---|
| REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN: RO FIFER | DATE: 10-90 |
| MATERIAL | CHECKED: Greg McAllister | 7-2-90 |
| | PROJ ENGR: L.E. FISH | 7-2-90 |
| | RELEASE APPROV.: L.E. FISH | 7-2-90 |
| FINISH: WAVETEK PROCESS | UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ± .XXX ± | |
| DO NOT SCALE DRAWING | | |

WAVETEK SAN DIEGO, CALIFORNIA

TITLE: SCHEMATIC, MOTHERBOARD

| SIZE | FSCM NO. | DWG. NO. | REV |
|---|---|---|---|
| D | 23338 | 1104-00-3395 | D |

SCALE: NONE | MODEL 90 SERIES | SHEET 1 OF 10

1104-00-3395 D B

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# MICRO PROCESS SECTION

R8 10k

+5V

C17 .1

U5 TL7705A

SENSE RESIN CT REF RESET RESET N/C

C18 22

C19 .1

C150 7-35pF

C20 15pF

C21 68pF NOM

Y1 4MHz

+5V C22 .1

U6 MC6803L

XTAL1 XTAL2 RESET E R/W AS P20 TIN P21 TOUT P22 SCLK P23 RX P24 TX P10 P11 P12 P13 P14 P15 P16 P17 NMI IRQ

AD0 P30 AD1 P31 AD2 P32 AD3 P33 AD4 P34 AD5 P35 AD6 P36 AD7 P37

A8 P40 A9 P41 A10 P42 A11 P43 A12 P44 A13 P45 A14 P46 A15 P47

R9 10k R10 10k R11 10k

SW1 39-405

DVM_BAT B5 F02

CR3 HP2811

R12 49.9k

R14 49.9k

Q11 VN10KM

R13 274

CR6 LTL-3231A

Q1 2N3904

P10 F01 D7

P11 F01 C7

P12 F01 D7

P13 F01 C7

P14 F01 D7

P15 F01 C7

P16 F01 D7

P17 F01 D7

CR4 HP2811

CR5 MBR120

R15 2.21k

BT1 BR2/3A

Q12 VN10KM

U11 HM6264LP-15

OE WE CS1 CS2 A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 I/O1 I/O2 I/O3 I/O4 I/O5 I/O6 I/O7 I/O8

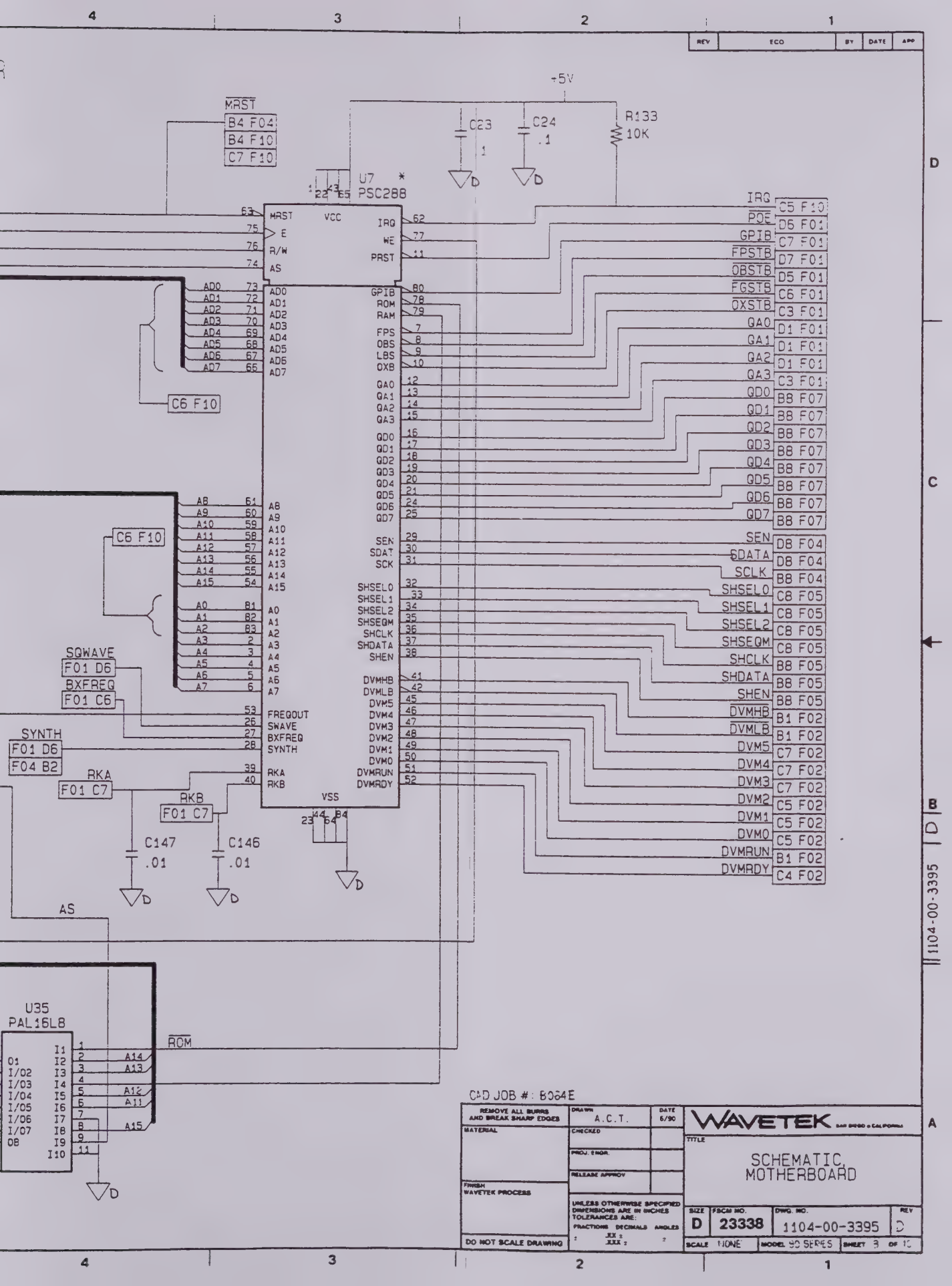
AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7

C29 .1

U12 *

CE OE/VPP A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 O0 O1 O2 O3 O4 O5 O6 O7

NOTE UNLESS OTHERWISE SPECIFIED


+5V
MRST
B4 F04
B4 F10
C7 F10
C23
1
C24
.1
R133
10K
U7 *
PSC288
MRST
E
R/W
AS
VCC
IRQ
WE
PRST
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
C6 F10
GPIB
ROM
RAM
FPS
OBS
LBS
OXB
GA0
GA1
GA2
GA3
GD0
GD1
GD2
GD3
GD4
GD5
GD6
GD7
SEN
SDAT
SCK
SHSEL0
SHSEL1
SHSEL2
SHSEQM
SHCLK
SHDATA
SHEN
DVMHB
DVMLB
DVM5
DVM4
DVM3
DVM2
DVM1
DVM0
DVMRUN
DVMRDY
A8
A9
A10
A11
A12
A13
A14
A15
A0
A1
A2
A3
A4
A5
A6
A7
FREQOUT
SWAVE
BXFREQ
SYNTH
RKA
RKB
VSS
SQWAVE
F01 D6
BXFREQ
F01 C6
SYNTH
F01 D6
F04 B2
RKA
F01 C7
RKB
F01 C7
C147
.01
C146
.01
AS
IRQ C5 F10
POE D6 F01
GPIB C7 F01
FPSTB D7 F01
OBSTB D5 F01
FGSTB C6 F01
OXSTB C3 F01
GA0 D1 F01
GA1 D1 F01
GA2 D1 F01
GA3 C3 F01
GD0 B8 F07
GD1 B8 F07
GD2 B8 F07
GD3 B8 F07
GD4 B8 F07
GD5 B8 F07
GD6 B8 F07
GD7 B8 F07
SEN D8 F04
SDATA D8 F04
SCLK B8 F04
SHSEL0 C8 F05
SHSEL1 C8 F05
SHSEL2 C8 F05
SHSEQM C8 F05
SHCLK B8 F05
SHDATA B8 F05
SHEN B8 F05
DVMHB B1 F02
DVMLB B1 F02
DVM5 C7 F02
DVM4 C7 F02
DVM3 C7 F02
DVM2 C5 F02
DVM1 C5 F02
DVM0 C5 F02
DVMRUN B1 F02
DVMRDY C4 F02
U35
PAL16L8
ROM
A14
A13
A12
A11
A15
CAD JOB #: B084E
A.C.T.
WAVETEK
SCHEMATIC,
MOTHERBOARD
SIZE D
FSCM NO. 23338
DWG. NO. 1104-00-3395
REV D
SCALE NONE
MODEL 90 SERIES
SHEET 3 OF 10
1104-00-3395

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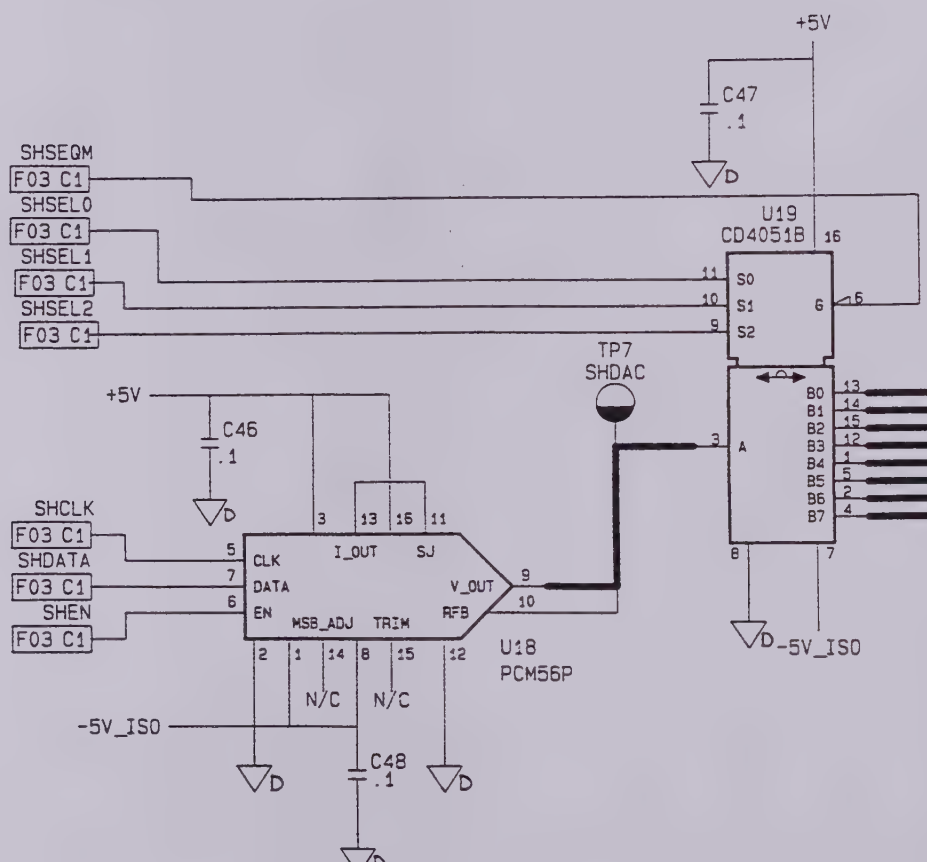
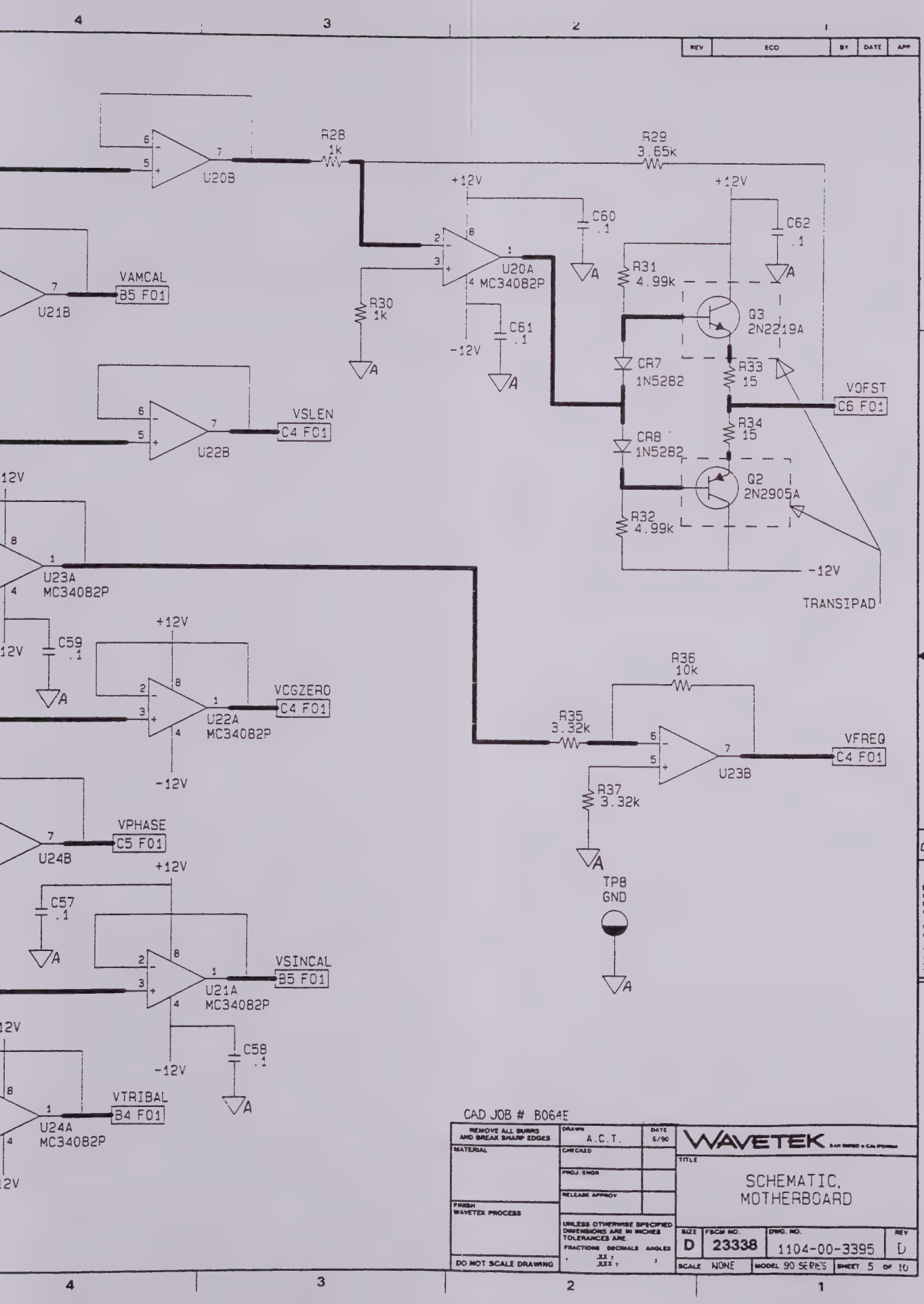
# DAC/SAMPLE AND HOLD NETWORK




NOTE UNLESS OTHERWISE SPECIFIED


REV
ECO
BY
DATE
APP
U20B
R28
1k
R29
3.65k
+12V
C60
.1
C62
.1
U20A
MC34082P
R31
4.99k
Q3
2N2219A
R30
1k
C61
.1
-12V
CR7
1N5282
R33
15
VOFST
C6 F01
CR8
1N5282
R34
15
Q2
2N2905A
R32
4.99k
-12V
TRANSIPAD
VAMCAL
B5 F01
U21B
VSLEN
C4 F01
U22B
U23A
MC34082P
C59
.1
VCGZERO
C4 F01
U22A
MC34082P
R36
10k
R35
3.32k
VFREQ
C4 F01
U23B
R37
3.32k
TP8
GND
VPHASE
C5 F01
U24B
C57
.1
VSINCAL
B5 F01
U21A
MC34082P
C58
.1
VTRIBAL
B4 F01
U24A
MC34082P
CAD JOB # B064E
REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DO NOT SCALE DRAWING
DRAWN A.C.T.
DATE 6/90
CHECKED
PROJ. ENGR
RELEASE APPROV
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
WAVETEK
TITLE
SCHEMATIC, MOTHERBOARD
SIZE D
FSCM NO. 23338
DWG. NO. 1104-00-3395
REV D
SCALE NONE
MODEL 90 SERIES
SHEET 5 OF 10
1104-00-3395

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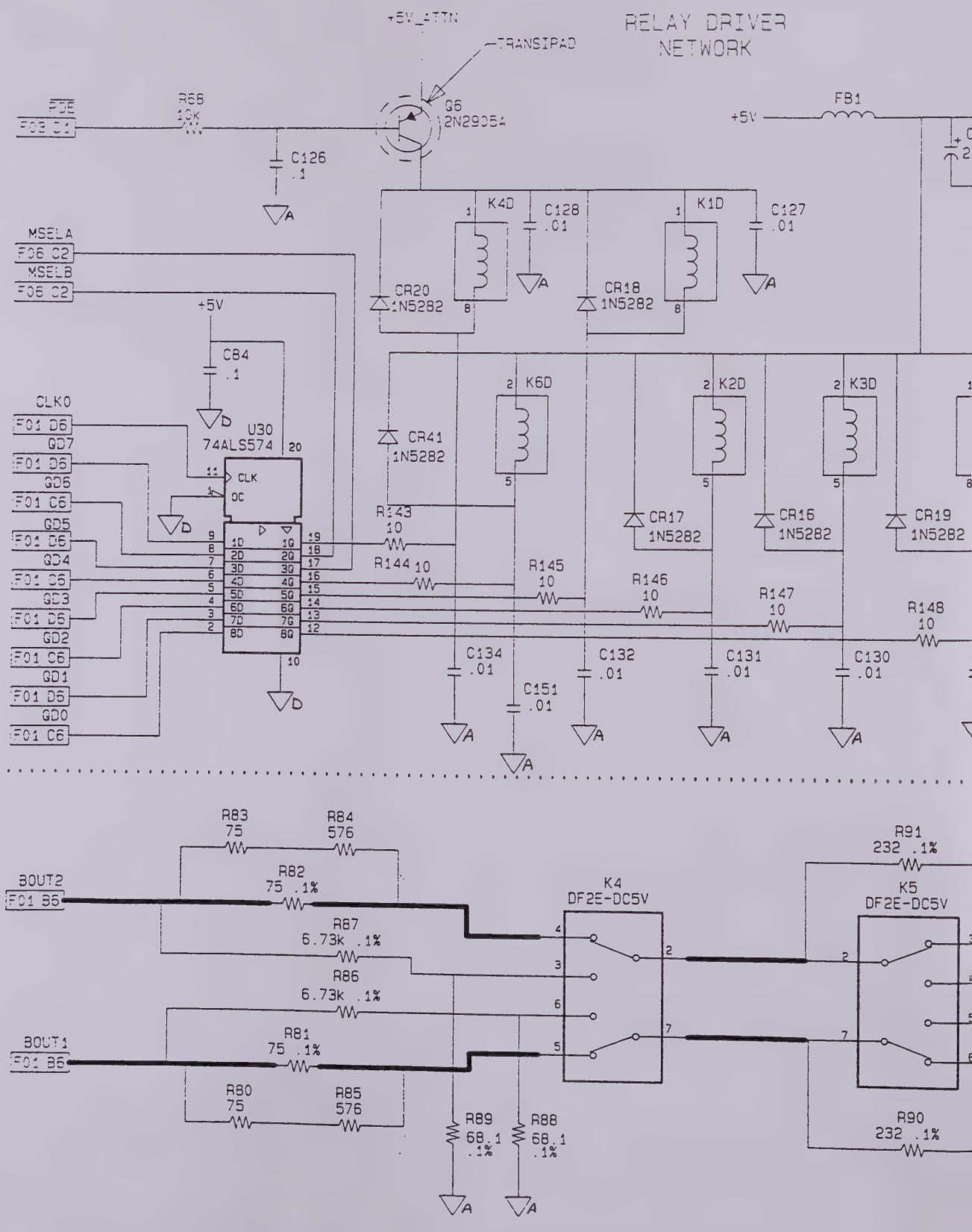
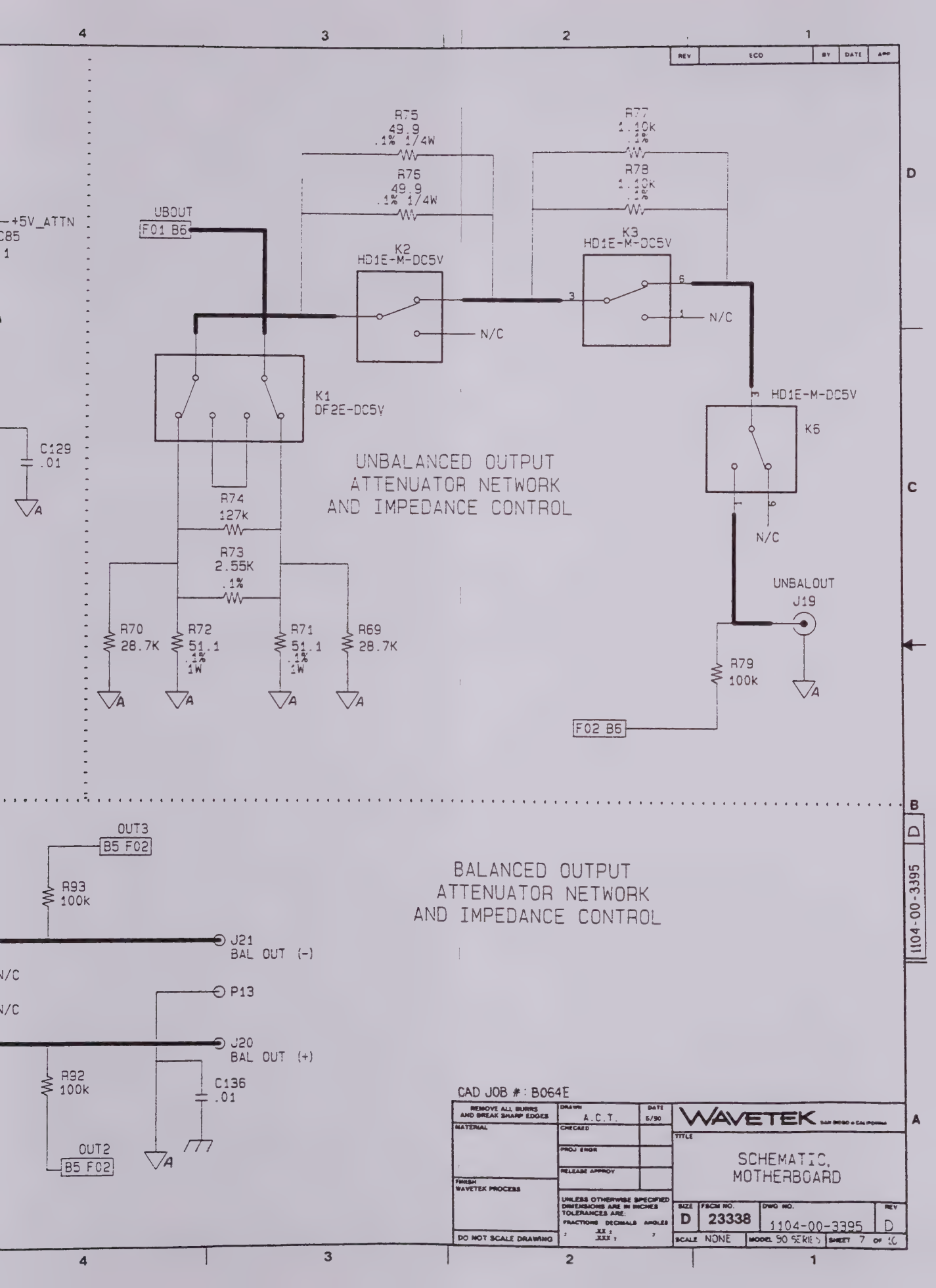
# RELAY DRIVER NETWORK




NOTE UNLESS OTHERWISE SPECIFIED


REV
ECO
BY
DATE
APP
R75
49.9
.1% 1/4W
R76
49.9
.1% 1/4W
R77
1.10k
.1%
R78
1.10k
.1%
UBOUT
F01 B6
K2
HD1E-M-DC5V
K3
HD1E-M-DC5V
N/C
N/C
K1
DF2E-DC5V
HD1E-M-DC5V
K6
N/C
UNBALANCED OUTPUT
ATTENUATOR NETWORK
AND IMPEDANCE CONTROL
C129
.01
R74
127k
R73
2.55K
.1%
R70
28.7K
R72
51.1
.1%
1W
R71
51.1
.1%
1W
R69
28.7K
UNBALOUT
J19
R79
100k
F02 B6
OUT3
B5 F02
R93
100k
J21
BAL OUT (-)
P13
J20
BAL OUT (+)
R92
100k
C136
.01
OUT2
B5 F02
BALANCED OUTPUT
ATTENUATOR NETWORK
AND IMPEDANCE CONTROL
1104-00-3395
CAD JOB # : B064E
REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH
WAVETEK PROCESS
DO NOT SCALE DRAWING
DRAWN
A.C.T.
DATE
5/90
CHECKED
PROJ ENGR
RELEASE APPROV
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
XX ±
XXX ±
WAVETEK
TITLE
SCHEMATIC,
MOTHERBOARD
SIZE
D
FSCM NO.
23338
DWG NO.
1104-00-3395
REV
D
SCALE NONE
MODEL 90 SERIES
SHEET 7 OF 10

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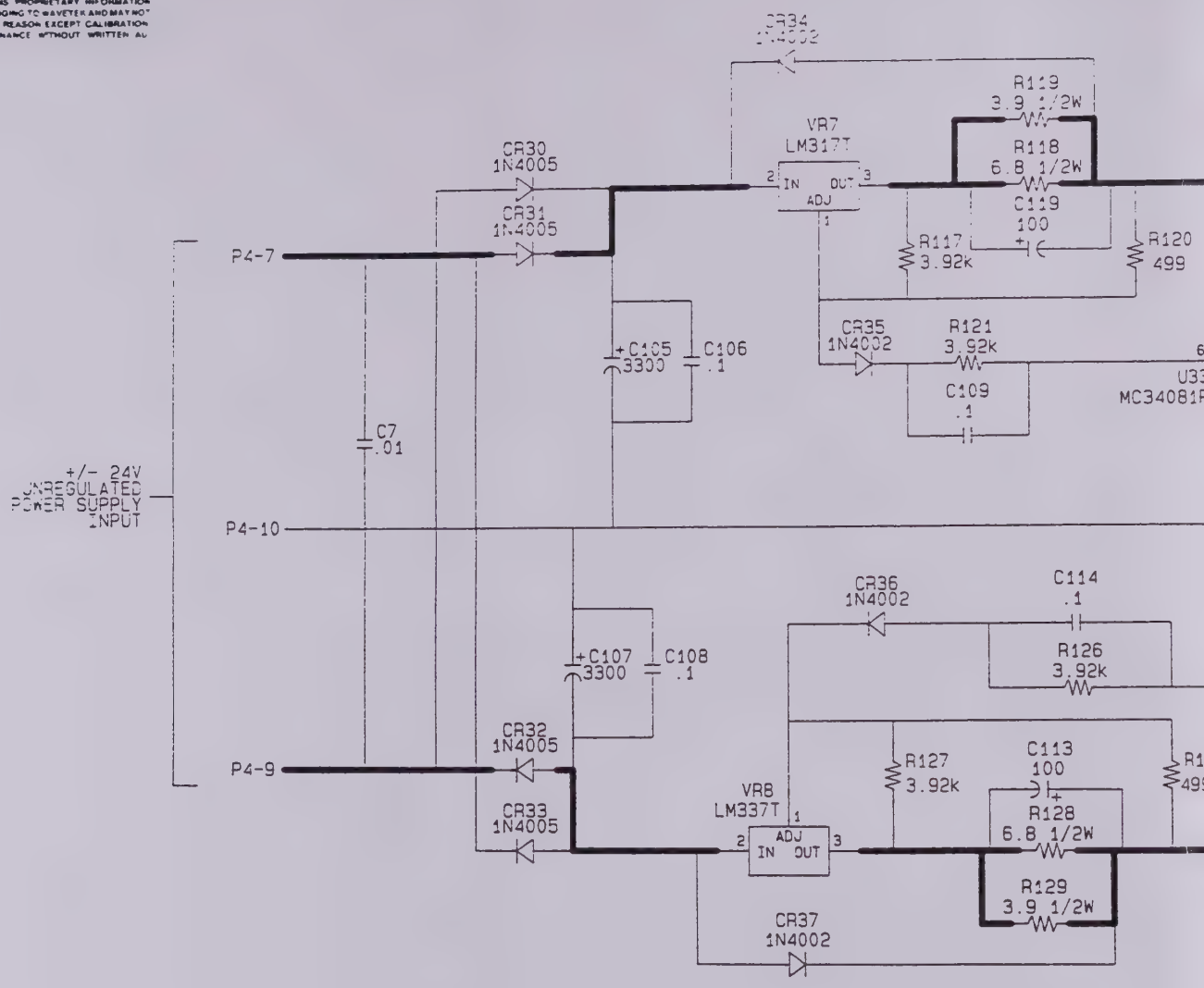
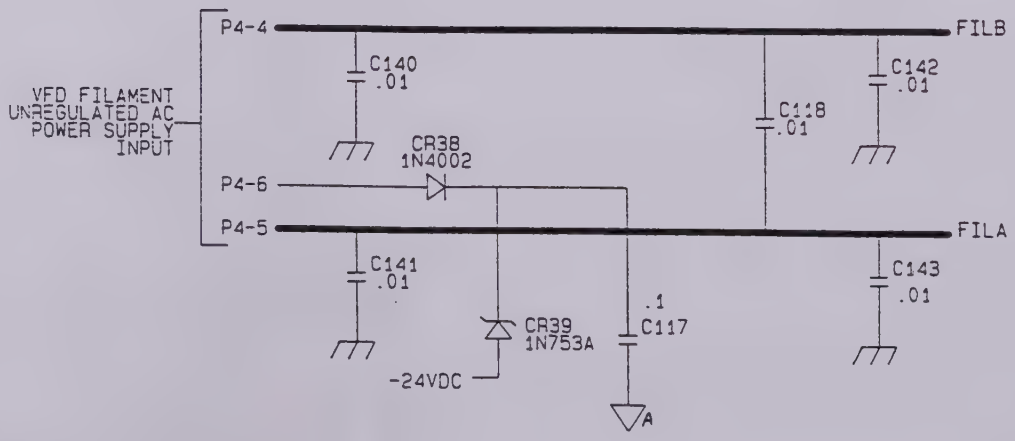


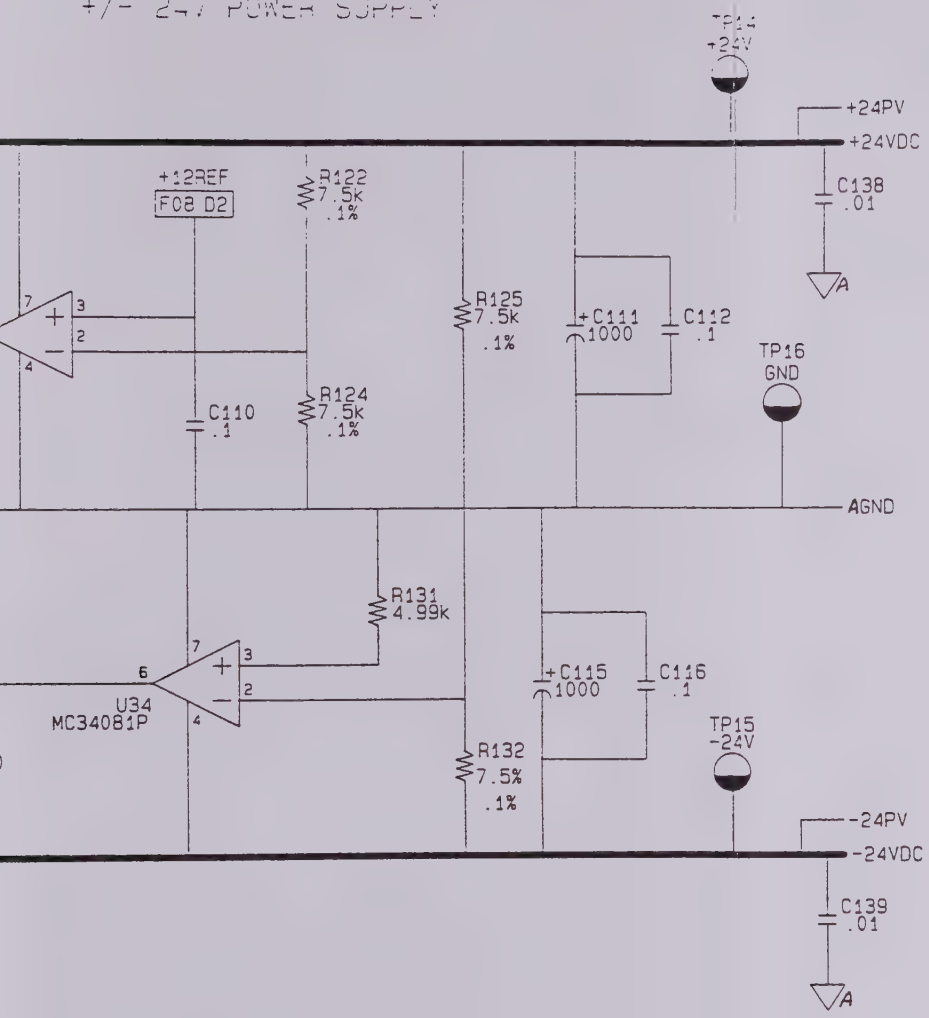

## VFD AC FILAMENT SUPPLY




NOTE UNLESS OTHERWISE SPECIFIED

| REV | ECO | BY | DATE | APP |
|---|---|---|---|---|

# +/- 24V POWER SUPPLY




CAD JOB #: B064E

| | | | |
|---|---|---|---|
| REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN A.C.T. | DATE 6/90 | WAVETEK San Diego, California |
| MATERIAL | CHECKED | | TITLE: SCHEMATIC, MOTHERBOARD |
| | PROJ. ENGR. | | |
| FINISH WAVETEK PROCESS | RELEASE APPROV. | | |
| DO NOT SCALE DRAWING | UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE. FRACTIONS DECIMALS ANGLES . XX ± .XXX ± ° | | SIZE D · FSCM NO. 23338 · DWG. NO. 1104-00-3395 · REV C · SCALE NONE · MODEL 90 SERIES · SHEET 4 OF 10 |

1104-00-3395

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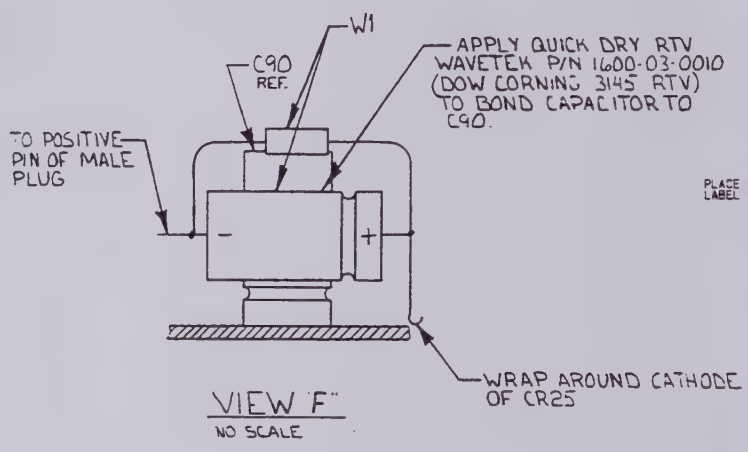
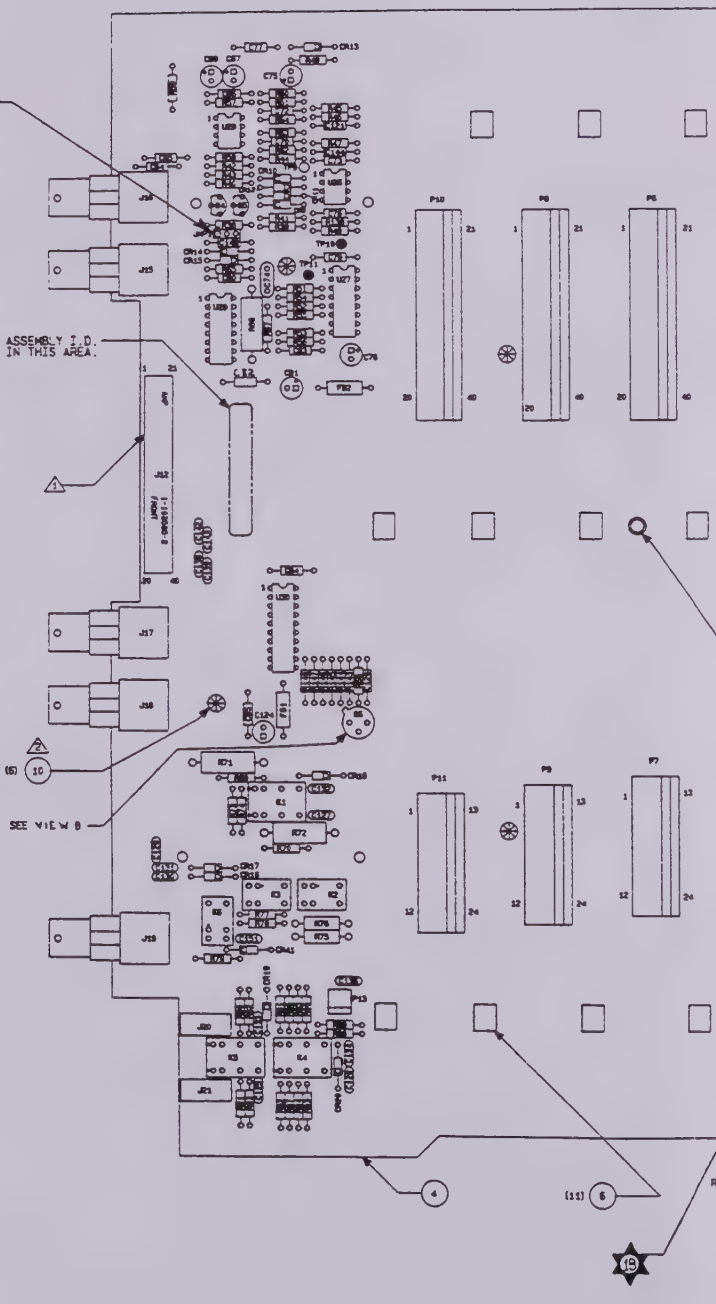

W1
C90 REF.
APPLY QUICK DRY RTV WAVETEK P/N 1600-03-0010 (DOW CORNING 3145 RTV) TO BOND CAPACITOR TO C90.
TO POSITIVE PIN OF MALE PLUG
WRAP AROUND CATHODE OF CR25

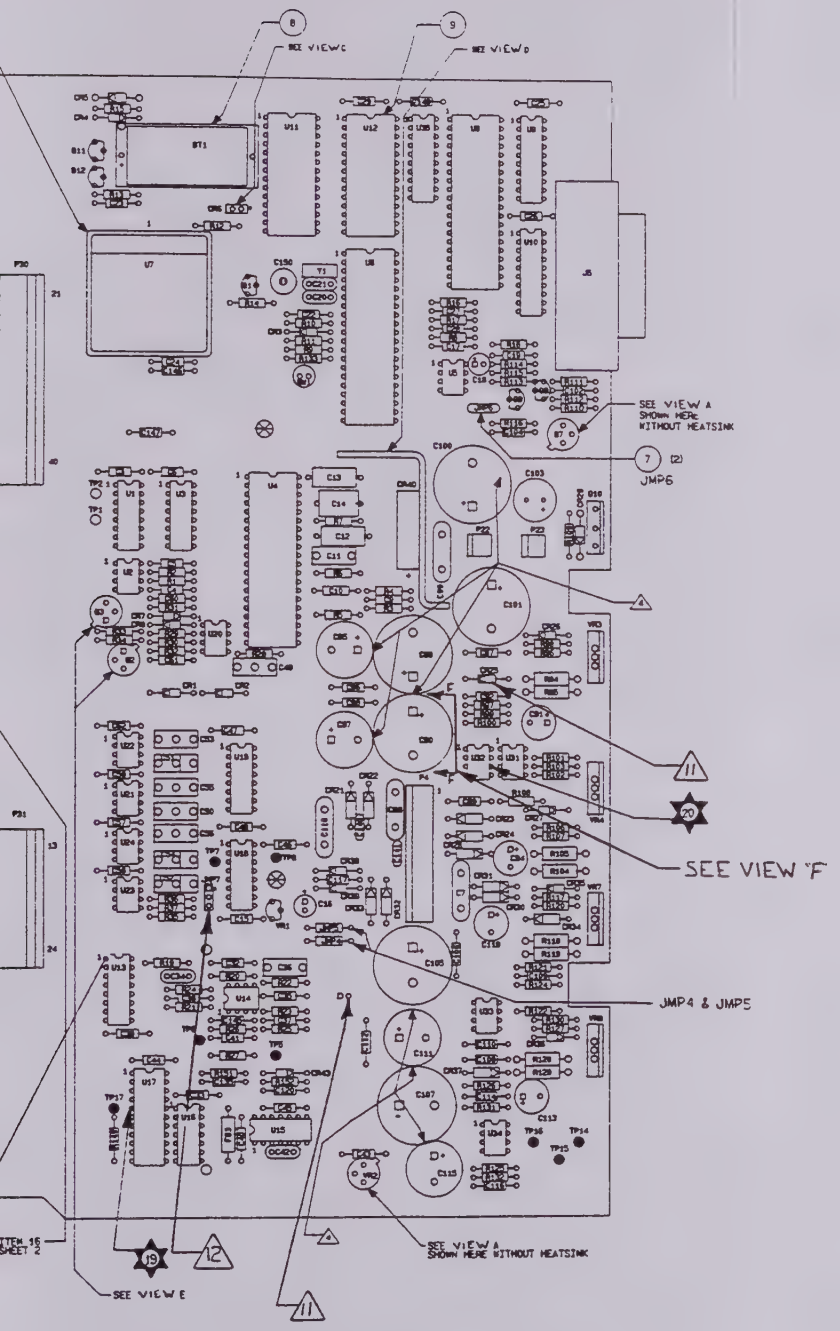
VIEW "F"
NO SCALE




13. INSTALL SHORTING JUMPER JMP1 BETWEEN PINS 1+2 (BIPOLAR CONFIGURATION).
12. INSTALL SHORTING JUMPER JMP7 ON PINS 1+2 FOR STD INSTRUMENT + PINS 2+3 FOR OPTION 001.
11. ATTACH FAN CABLE ASSY, W1, AS FOLLOWS. (SEE VIEW "F")
    A. RESISTOR / CAPACITOR END OF W1 TO CATHODE OF CR25.
    B. BLACK WIRE END OF W1 TO GND HOLE AS SHOWN.
    C. SECURE CAPACITOR TO C90 WITH RTV.
10. ASSEMBLE PER WAVETEK WORKMANSHIP STANDARDS.
9. REFERENCE DESIGNATIONS DO NOT APPEAR ON PARTS.
8. FOR ASSEMBLY INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 1004-00-0596 FOR MODEL 90 AND 1004-00-0599 FOR MODEL 95.
7. SEE 1104-00-3395 FOR SCHEMATIC.
6. COMPONENTS UNDER ITEM NO. 19 TO BE .465 MAX FROM SURFACE OF BOARD.
5. COMPONENTS UNDER ITEM NO. 18 TO BE .325 MAX FROM SURFACE OF BOARD.
4. INSTALL CLEAR RTV BETWEEEN CAPACITORS: C115-C107, C107-C111, C111-C105, C97-C90, C90-C88, C88-C95, C103-C100.
3. INSTALL CANS FLUSH TO COMPONENT SIDE OF P.C. BOARD. SOLDER TABS TO CIRCUIT SIDE.
2. ITEM 10 (SPACERS) TO BE INSTALLED FROM BOTTOM SIDE OF BOARD (CIRCUIT SIDE).
1. MANUFACTURER'S MARKING INDICATES CORRECT ORIENTATION OF CONNECTOR.

NOTE UNLESS OTHERWISE SPECIFIED

| REV | ECO | BY | DATE | APP |
|---|---|---|---|---|
| A | ECO NO 90-481 | DL | [illegible] | [illegible] |
| B | ECO # 90-506 | MS | 4/24/90 | [illegible] |
| C | ECO # 90-521 | MS | 5/12/90 | [illegible] |
| D | ECO # 90-5[illegible]1 | MS | [illegible] | [illegible] |
| E | ECO # 91-116 | [illegible] | 1/31/91 | |




CAD JOB #: B064E

| | | |
|---|---|---|
| REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN Amy Talmadge | DATE 6/20/90 |
| MATERIAL | CHECKED D. FISH | 6/20/90 |
| | PROJ ENGR [signature] | 6/29/90 |
| FINISH WAVETEK PROCESS | RELEASE APPROV [signature] | 6/20/90 |
| DO NOT SCALE DRAWING | UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ± .01 .XXX ± .005 | |

WAVETEK SAN DIEGO, CALIFORNIA

TITLE: PCA, MOTHERBOARD

| SIZE | FSCM NO. | DWG NO | REV |
|---|---|---|---|
| D | 23338 | 1101-00-3395 | E |

SCALE FULL | MODEL 90 SERIES | SHEET 1 OF 1

1101-00-3395 E

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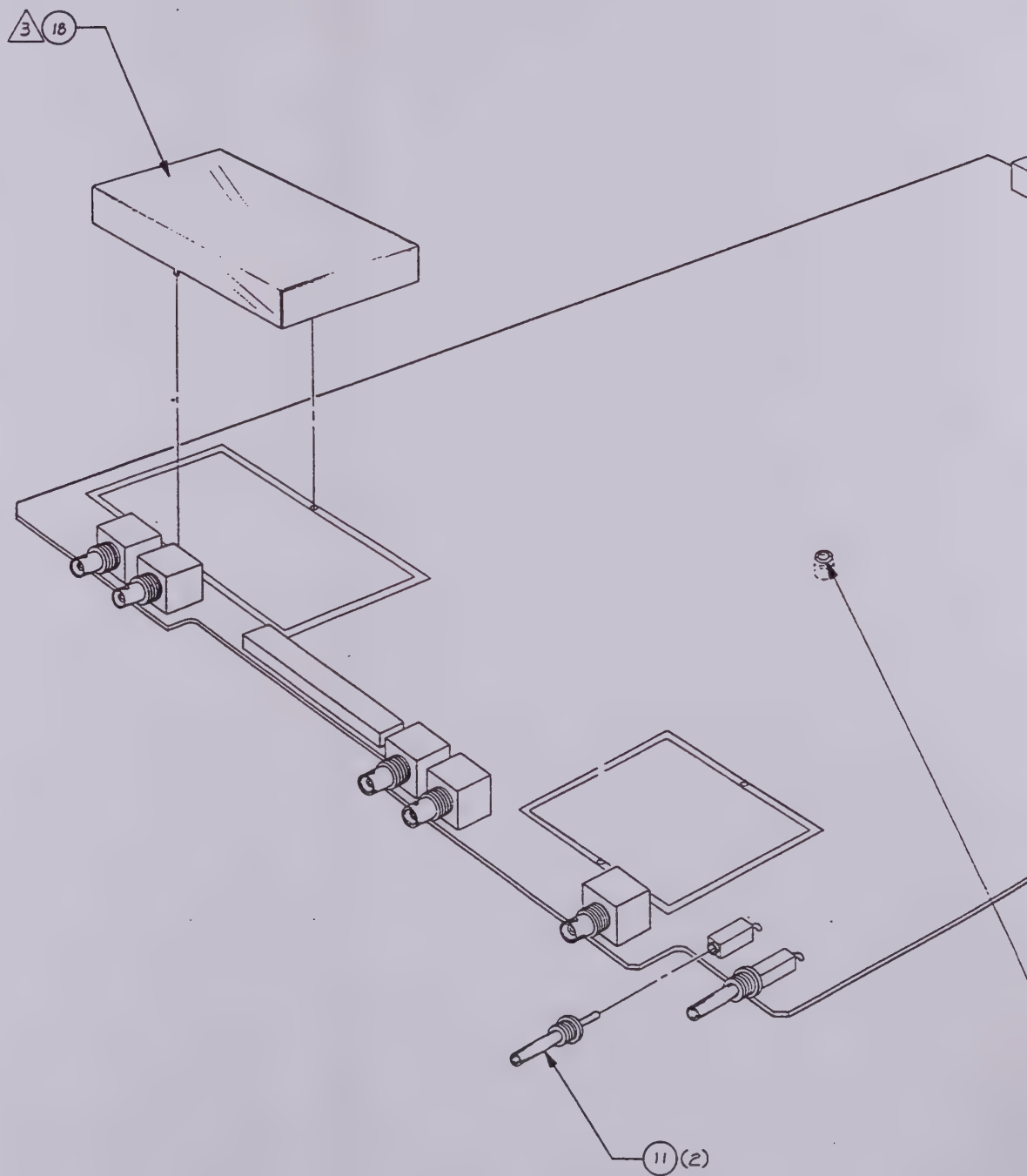
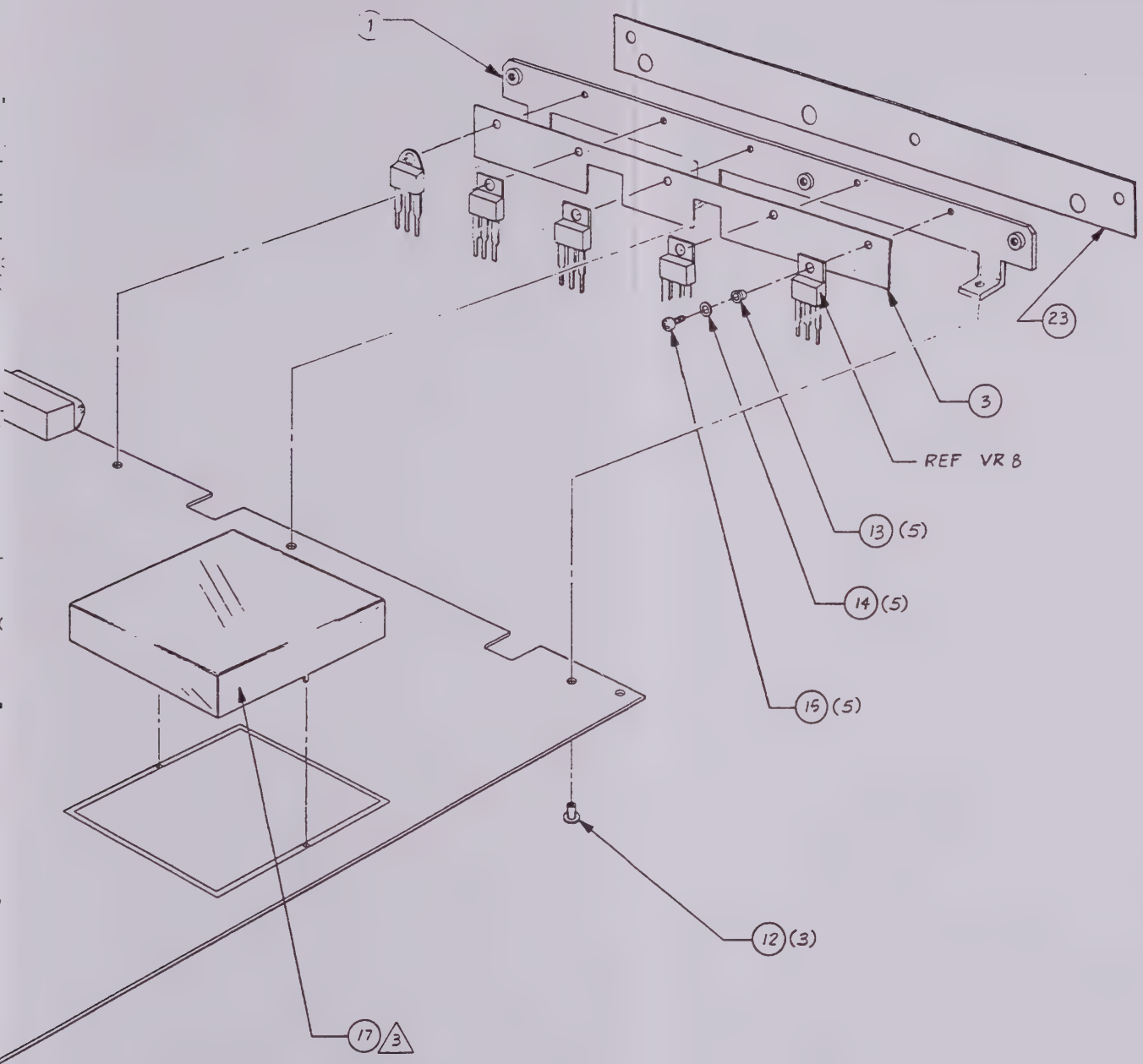



NOTE: UNLESS OTHERWISE SPECIFIED

| REV | ECN | BY | DATE | APP |
|---|---|---|---|---|

SEE SHEET 1




16 INSTALL SWAGE STANDOFF FROM CIRCUIT SIDE OF BOARD.

| | | | |
|---|---|---|---|
| REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN S CHERMACK | DATE 6/20/90 | WAVETEK SAN DIEGO, CALIFORNIA |
| MATERIAL | PROJ ENGR | | TITLE PCA, MOTHERBOARD |
| | RELEASE APPROV | | |
| FINISH WAVETEK PROCESS | TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1° XX ±.030 | | |
| | DO NOT SCALE DWG | MODEL NO 90 SERIES | DWG NO 1101-00-3395 REV E |
| | SCALE NONE | CODE IDENT 23338 | SHEET 3 OF 3 |

A 3 2 1

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION OPERATION AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION

| REFERENCE DESIGNATORS | PART DESCRIPTION |
|---|---|
| NONE | A/D MOTHER BD 90/95 |
| NONE | SCHEMATIC, MOTHER BD 90/95 |
| NONE | 90/95 MOTHERBOARD PREWAVE LOAD |
| W1 | FAN CABLE ASSY |
| 17 | CAN, SYNTHESIZER |
| 18 | CAN, FREQ IN/SYNC OUT |
| 3 | THERMAL GASKET-REAR PANEL-A |
| 23 | THERMAL GASKET-REAR PANEL-B |
| 28 | HEATSINK BRIDGE |
| 1 | SUPPPORT PLATE, TRANSISTOR |
| J15 J16 J17 J18 J19 | CONN, BNC(PC) |
| XJMP1 | CONN, HEADER, 3 PIN |
| JMP1 JMP7 | JUMPER, FEMALE, 2 POSITION, 0.1 SPACE |
| 20 | HEAT SINK |

WAVETEK PARTS LIST

TITLE
PCA, MOTHER BOARD

NOTE UNLESS OTHERWISE SPECIFIED

D C B A

8 7 6 5

| REV | ECO | BY | DATE | APP |
|---|---|---|---|---|

| ORIG-MFGR-PART-NO | MFGR | WAVETEK NO | QTY/PT |
|---|---|---|---|
| 1101-00-3483 | WVTK | 1101-00-3483 | 1 |
| 1104-00-3483 | WVTK | 1104-00-3483 | 1 |
| 1200-00-3390 | WVTK | 1200-00-3390 | 1 |
| 1200-00-3429 | WVTK | 1200-00-3429 | 1 |
| 1400-02-3443 | WVTK | 1400-02-3443 | 1 |
| 1400-02-3453 | WVTK | 1400-02-3453 | 1 |
| 1400-02-4400 | WVTK | 1400-02-4400 | 1 |
| 1400-02-4410 | WVTK | 1400-02-4410 | 1 |
| 1400-02-4463 | WVTK | 1400-02-4463 | 1 |
| 1400-02-5007 | WVTK | 1400-02-5007 | 1 |
| 227161-1 | AMP | 2100-01-0019 | 5 |
| 929834-01-03 | APTRN | 2100-02-0196 | 1 |
| 929950-00 | APTRN | 2100-02-0213 | 2 |
| 207 | WAKE | 2800-11-0001 | 2 |

| | ASSEMBLY NO. 1100-00-3395 | REV K |
|---|---|---|
| | PAGE 1 | |

| REFERENCE DESIGNATORS | PART DESCRIPTION | ORIG-MFGR-PART-NO | MFGR | WAVETEK NO | QTY/PT |
|---|---|---|---|---|---|
| 13 | WASHER | 9607-150 | SESTM | 2800-11-0015 | 5 |
| 12 | RIVET, 1/8 BODY DIA. 1/8-3/16 GRIP SS | SSD439SBS | EMHRT | 2800-12-0035 | 3 |
| 25 | NUT, HEX, 6-32, Z | MS35649-264 | COML | 2800-14-6100 | 1 |
| 26 | WASHER #6 SAE FLAT, .375 O.D. | 6 SAE FLAT WASHER | CMRCL | 2800-26-6000 | 1 |
| 10 | HOLE PLUG, BINDER HEAD, NTRAL NYLON | 207-120241-03-0101 | FASTX | 2800-35-0009 | 6 |
| 27 | #6 LOCKWASHER, PLATED | #6SRLW | CMRCL | 2800-42-6000 | 1 |
| 14 | WASHER, LOCK REC, S/S #4 | MS 35338-135 | CMRCL | 2800-45-4000 | 5 |
| 15 | SCREW PLPS PAN M/S 18-8 S/S 4-40X1/4 | MS 51957-13 | CMRCL | 2800-48-4104 | 5 |
| 24 | SCREW, PH, PHLPS, 6-32X9 /16, SS | 2800-61-6109 | CMCRL | 2800-61-6109 | 1 |
| Q10 | TRANS | TIP-36 | TI | 4902-00-0360 | 1 |
| VR3 VR7 | VOLT REGULATOR, 3 TERMINAL ADJUSTABLE POS | LM317T | NSC | 7000-03-1700 | 2 |
| VR4 VR8 | VOLT REGULATOR | LM337T | NSC | 7000-03-3700 | 2 |

| WAVETEK PARTS LIST | TITLE PCA, MOTHER BOARD | ASSEMBLY NO. 1100-00-3395 | REV K |
|---|---|---|---|
| | | PAGE 2 | |

| REFERENCE DESIGNATORS | PART DESCRIPTION | ORIG-MFGR-PART-NO | MFGR | WAVETEK NO. | QTY/PT |
|---|---|---|---|---|---|
| 6U12 | EPROM PROG USEA 1 EA 8002-73-1200 FOR MOD 90 V 1.3 REF U12 | 8600-00-0635 | WVTK | 8600-00-0635 | 1 |

| WAVETEK PARTS LIST | TITLE PCA, MOTHER BOARD | ASSEMBLY NO. 1100-00-3395 | REV K |
|---|---|---|---|
| | | PAGE 3 | |

| REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN | DATE |
|---|---|---|
| MATERIAL | CHECKED | |
| | PROJ. ENGR. | |
| | RELEASE APPROV. | |
| FINISH WAVETEK PROCESS | UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ± XX ± .XXX ± ° | |
| DO NOT SCALE DRAWING | | |

WAVETEK San Diego, California

TITLE

PARTS LIST
MOTHERBOARD

| SIZE | FSCM NO. | DWG NO. | REV |
|---|---|---|---|
| D | 23338 | 1100-00-3395 | K |
| SCALE | MODEL 90 | SHEET 1 OF 1 | |

4 3 2 1

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| REFERENCE DESIGNATORS | PART DESCRIPTION | ORIG-MFGR-PART-NO | MFGR | WAVETEK NO | QTY/PT |
|---|---|---|---|---|---|
| VR1 | G N V REG 5V (79L05) | LM320LZ-5 0 | NSC | 120 0054 | 1 |
| CR39 CR43 | SL ZR 6 2V 5% 400MW (1N753A) | 1N753A | RDMM | 131 9620 | 2 |
| C74 | CAP CER MON 100PF 50V COG 5% RAD LD SP .2 | 5028E050RD101J | KYCRA | 1500-01-0103 | 1 |
| C41 | CAP,CER, .001MF, 100V | SA101C102MAATR | AVX | 1500-01-0206 | 1 |
| C118 C7 C86 C99 | CAP,CER, 01MF,1KV | CAP-103 | CRL | 1500-01-0309 | 4 |
| C146 C147 | CAP CER MON 01MF 50V, AXIAL | CAC02Z5U103Z100A | CORNG | 1500-01-0310 | 2 |
| C127 C128 C129 C130 C131 C132 C133 C134 C136 C138 C139 C140 C141 C142 C143 C151 C34 | CAP CER MON 01MF 50V Z5U +80/-20% RAD LD .2 | 1C20Z5U103M050B | SPRAG | 1500-01-0311 | 17 |
| C102 C104 C106 C108 C109 C110 C112 C114 C116 C117 C120 C126 C135 C145 C149 C15 C17 C19 C22 C23 C24 C25 C26 C27 C28 C3 C32 C33 C37 C38 C39 C4 C40 C43 C44 C45 C46 C47 C48 C5 C57 C58 C59 C6 C60 C61 C62 C64 C65 C66 C70 C72 C73 C76 C77 C79 C80 C82 C83 C84 C85 C87 C89 C91 C92 C96 C98 | CAP,CER,MON, 1MF,50V, AXIAL | CAC03Z5U104Z050A | CORNG | 1500-01-0405 | 67 |

| WAVETEK PARTS LIST | TITLE 90/95 MOTHERBOARD PREWAVE LOAD | ASSEMBLY NO. 1200-00-3390 | REV E |
|---|---|---|---|

PAGE 1

| REFERENCE DESIGNATORS | PART DESCRIPTION |
|---|---|
| C124 C16 C18 C67 C68 C75 C78 | CAP,ELECT,22MF,25V,RADIAL |
| C95 C97 | CAP,ELECT,2200MF,16V RADIAL LEAD, SP .30 |
| C105 C107 | CAP,ELECT,3300MF,50V RADIAL LEAD, SP .40 |
| C88 C90 | CAP,ELECT,4700MF/25V RADIAL LEAD, SP .30 |
| C100 C101 | CAP, ELECT, 16V, 6800 uF, RAD, 0.4 LS |
| C14 | CAP,POLYC,.01MF,100V, AXIAL |
| C11 C36 C49 C50 C53 C55 C56 | C05 CAP,MET POLY,.1MF,100V/160V DC,.4 LS |
| C13 | CAP,MYLAR,1MF,100V,RADIAL |
| C51 C52 C54 | CAP,MET-POLY,5% 47MF, 63V RADIAL LEAD SP .2 |
| C12 | CAP,POLYPRO,.056MF,200V,2%,AXIAL |
| C150 | CAP,VAR, 7-35PF 250V |

| WAVETEK PARTS LIST | TITLE 90/95 MOTHERBOARD PREWAVE |
|---|---|

| REFERENCE DESIGNATORS | PART DESCRIPTION | ORIG-MFGR-PART-NO | MFGR | WAVETEK NO. | QTY/PT |
|---|---|---|---|---|---|
| C20 | CAP CER MON 15PF 50V COG 5% RADIAL LD SP .2 | 5028E050RD150J | KYCRA | 1500-01-0003 | 1 |
| C10 | CAP,CER,220PF,100V,AXIAL | CAC02CDG221J100A | CORNG | 1500-02-2106 | 1 |
| C42 | CAP CER MON 33PF 50V COG 5% RAD LD .2 | 5028E050RD330J | KYCRA | 1500-03-3020 | 1 |
| C148 | CAP,CER,330PF,100V,AXIAL | CAC02CDG331J100A | CORNG | 1500-03-3106 | 1 |
| C35 | CAP,CER,3300PF,100V,2%,AXIAL | CAC02X7R332M100A(OBS) | CORNG | 1500-03-3206 | 1 |
| C121 | CAP,CER,5.1PF,200V,AXIAL | SA102A5R1DAA | AVX | 1500-05-1906 | 1 |
| C21 | CAP,CERAMIC,68PF,100V ,5%,RAD LEAD .2 | SR211A680JAA | AVX | 1500-06-8016 | 1 |
| C113 C119 C91 C94 | CAP,ELECT,100MF,35V RADIAL LEAD,SP .20 | NRE101M35V10X12.5(OBS) | NIC | 1500-31-0102 | 4 |
| C111 C115 | CAP,ELECT,1000MF/50V RADIAL LEAD, SP .30 | NRE102M50V16X25 | NIC | 1500-31-0203 | 2 |
| C103 | CAP,ELECT,1000MF/16V RADIAL LEAD, SP .20 | 1500-31-0214 | WVTK | 1500-31-0211 | 1 |
| C81 | CAP,ELECT,220MF/10V | ECEA1AU221 | PANAS | 1500-32-2001 | 1 |

| WAVETEK PARTS LIST | TITLE 90/95 MOTHERBOARD PREWAVE LOAD | ASSEMBLY NO. 1200-00-3390 | REV E |
|---|---|---|---|

PAGE 2

| REFERENCE DESIGNATORS | PART DESCRIPTION |
|---|---|
| NONE | PCB,MOTHER BD REF: SPEC 0008-00-0435 REV E |
| P4 | CONN,HEADER |
| J20 J21 | PC JACK |
| NONE | CONN,HEADER, 3 PIN |
| J12 | CONN,HEADER,40 PIN,RECPT,2X20,.1 CTR PCMT |
| P11 P31 P7 P9 | CONN,HEADER,24 PIN,PCMT, .1 CTR,2X12,SHRD |
| P10 P30 P6 P8 | CONN,HEADER,40 PIN,PCB MT, .1 CTR,2X20,SHRD |
| J5 | CONN,RECP,GPIB,24POS, .125 TAIL,RT ANG,PC MT |
| 9 | SOCKET, IC, 28 PIN |
| 5 | SOCKET,84 PIN,PLCC,THRU HOLE |
| 7 | JACK,CLSD ENTRY,PCB TYPE,PRES MNT, 0.040 |

| WAVETEK PARTS LIST | TITLE 90/95 MOTHERBOARD PREWAVE |
|---|---|

NOTE UNLESS OTHERWISE SPECIFIED

8 7 6 5

| REV | ECO | BY | DATE | APP |
|---|---|---|---|---|

| RIG-MFGR-PART-NO | MFGR | WAVETEK NO | QTY/PT |
|---|---|---|---|
| RA25VB22RM6X7LL | UNCON | 1500-32-2002 | 7 |
| CEA1CV222SC | PANAS | 1500-32-2201 | 2 |
| RE332M50V22X41 | NIC | 1500-33-3202 | 2 |
| RSA472M25V18X36 | NIC | 1500-34-7202 | 2 |
| RE682M16V22X41 | NIC | 1500-36-8201 | 2 |
| 31B103F | BISHO | 1500-41-0304 | 1 |
| 500-41-0445 | WVTK | 1500-41-0434 | 7 |
| MT2R1.0K100 | ITT | 1500-41-0524 | 1 |
| 68474J63F | MALRY | 1500-44-7413 | 3 |
| A1C563-C | IMB | 1500-45-6300 | 1 |
| S-TRIKO-02 7/35PF(OBS | TRIKO | 1500-53-5000 | 1 |

| | ASSEMBLY NO. 1200-00-3390 | REV E |
|---|---|---|
| | PAGE 3 | |

| REFERENCE DESIGNATORS | PART DESCRIPTION | ORIG-MFGR-PART-NO | MFGR | WAVETEK NO | QTY/PT |
|---|---|---|---|---|---|
| | PIN | | | | |
| P13 P22 P23 | TERMINAL TAB (FASTON) | 62747-1 | AMP | 2100-04-0038 | 3 |
| TP11 TP16 TP2 TP6 TP8 | TEST POINT, BLK, PC | TP-104-01-00 | COMPD | 2100-04-0054 | 5 |
| TP1 TP10 TP14 TP15 TP17 TP5 TP7 TP9 | TEST POINT, RED, PC | TP-104-01-02 | COMPD | 2100-04-0055 | 8 |
| 11 | CONN PIN, INSERT | 2100-05-0061 | WVTK | 2100-05-0061 | 2 |
| Y1 | CRYSTAL, 4MHZ | 2532.000(REF ONLY) | MTRON | 2300-99-0004 | 1 |
| 6 | FUSE HOLDER, CLIP | 102071 | LITFU | 2400-05-0031 | 11 |
| 16 | STANDOFF, SW, 6-32X5/32 .1/16 SW, BR, ZN PL | 3045-B-632-B MODL-5/32 | RAF | 2800-06-0062 | 1 |
| 22 | TRANSIPAD | 503-075 | BIVAR | 2800-11-0003 | 1 |
| 21 | TRANSIPAD | 531-218 | BIVAR | 2800-11-0004 | 2 |
| JMP6 | JUMPER | 461-2871-01-03-10 | CAMBN | 3000-00-0034 | 1 |
| NONE | BATTERY HOLDER | BH 2/3A | MPD | 3000-00-0137 | 1 |
| FB1 FB2 FB3 | BALUN CORE, FERRITE, 680 OHMS | 2943666671 | FARIT | 3100-00-0017 | 3 |
| BT1 | BATTERY, 3V LITHIUM | BR-2/3A | PANAS | 4000-02-0008 | 1 |
| K1 K4 K5 | RELAY, 2 FORMC, 5V, DIP 14 | DF2E-DC5V | AROMT | 4500-00-0033 | 3 |

| WAVETEK PARTS LIST | TITLE 90/95 MOTHERBOARD PREWAVE LOAD | ASSEMBLY NO. 1200-00-3390 | REV E |
|---|---|---|---|
| | | PAGE 5 | |

| RIG-MFGR-PART-NO | MFGR | WAVETEK NO. | QTY/PT |
|---|---|---|---|
| 700-00-3395 | WVTK | 1700-00-3395 | 1 |
| -640386-0 | AMP | 2100-02-0079 | 1 |
| 9-9094-1-04 | CONCD | 2100-02-0190 | 2 |
| 29834-01-03 | APTRN | 2100-02-0196 | 1 |
| -0102585-2(REF ONLY) | AMP | 2100-02-0256 | 1 |
| 02692-2 | AMP | 2100-02-0257 | 4 |
| -102692-3 | AMP | 2100-02-0258 | 4 |
| 88-2R4-248M32X9 | BURND | 2100-02-0259 | 1 |
| ILB28P-108T | BURND | 2100-03-0081 | 1 |
| 21573-1 | AMP | 2100-03-0094 | 1 |
| 50-3752-01-06-00 | CAMB | 2100-03-0096 | 2 |

| | ASSEMBLY NO. 1200-00-3390 | REV E |
|---|---|---|
| | PAGE 4 | |

| REFERENCE DESIGNATORS | PART DESCRIPTION | ORIG-MFGR-PART-NO | MFGR | WAVETEK NO. | QTY/PT |
|---|---|---|---|---|---|
| K2 K3 K6 | RELAY, 1 FORMC, 5V, .312H, .296W | MD1E-M-DC5V | AROMT | 4500-00-0034 | 3 |
| R104 R105 R94 R95 | RES, C, 1/2W, 5%, 1.8 | RC-1/2-1R8J | STKPL | 4700-25-0189 | 4 |
| R119 R129 | RES, C, 1/2W, 5%, 3.9 | RC-1/2-3R9J | STKPL | 4700-25-0399 | 2 |
| R118 R128 | RES, C, 1/2W, 5%, 6.8 | RC-1/2-6R8J | STKPL | 4700-25-0689 | 2 |
| R112 R114 R115 | RES, MF, 1/8W, .1%, 1K | RN55E-1001B | MEPCO | 4701-02-1001 | 3 |
| R100 | RES, MF, 1/8W, .1%, 10K | RN55E-1002B | MEPCO | 4701-02-1002 | 1 |
| R77 R78 | RES, MFLM, 1/8W, .1%, 1.1K | 5033RE1101B | MEPCO | 4701-02-1101 | 2 |
| R2 | RES, MF, 1/8W, .1%, 1.5K | RN55E-1501B | CORNC | 4701-02-1501 | 1 |
| R99 | RES, MF, 1/8W, .1%, 2K | RN55E-2001B | MEPCO | 4701-02-2001 | 1 |
| R90 R91 | RES, MFLM, 1/8W, .1%, 232 | 5033RE2320B | MEPCO | 4701-02-2320 | 2 |
| R73 | RES, MFLM, 1/8W, .1%, 2.55K | 5033RE2551B | MEPCO | 4701-02-2551 | 1 |
| R1 R111 R3 | RES, MF, 1/8W, .1%, 3K | RN55E-3001B | MEPCO | 4701-02-3001 | 3 |
| R86 R87 | RES, MFLM, 1/8W, .1%, 6.73K | 5033RE6731B | MEPCO | 4701-02-6731 | 2 |
| R88 R89 | RES, MFLM, 1/8W, .1%, 68.1 | CMF-5568R1BT-9 | DALE | 4701-02-6819 | 2 |

| WAVETEK PARTS LIST | TITLE 90/95 MOTHERBOARD PREWAVE LOAD | ASSEMBLY NO 1200-00-3390 | REV E |
|---|---|---|---|
| | | PAGE 6 | |

| | | | |
|---|---|---|---|
| REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN | DATE | WAVETEK SAN DIEGO, CALIFORNIA |
| MATERIAL | CHECKED | | TITLE PARTS LIST MOTHERBOARD PREWAVE |
| | PROJ. ENGR. | | |
| | RELEASE APPROV. | | |
| FINISH WAVETEK PROCESS | UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ± .XXX ± | | SIZE D FSCM NO. 23338 DWG. NO. 1200-00-3390 REV E |
| DO NOT SCALE DRAWING | | | SCALE MODEL 90 SHEET 1 OF 2 |

4 3 2 1

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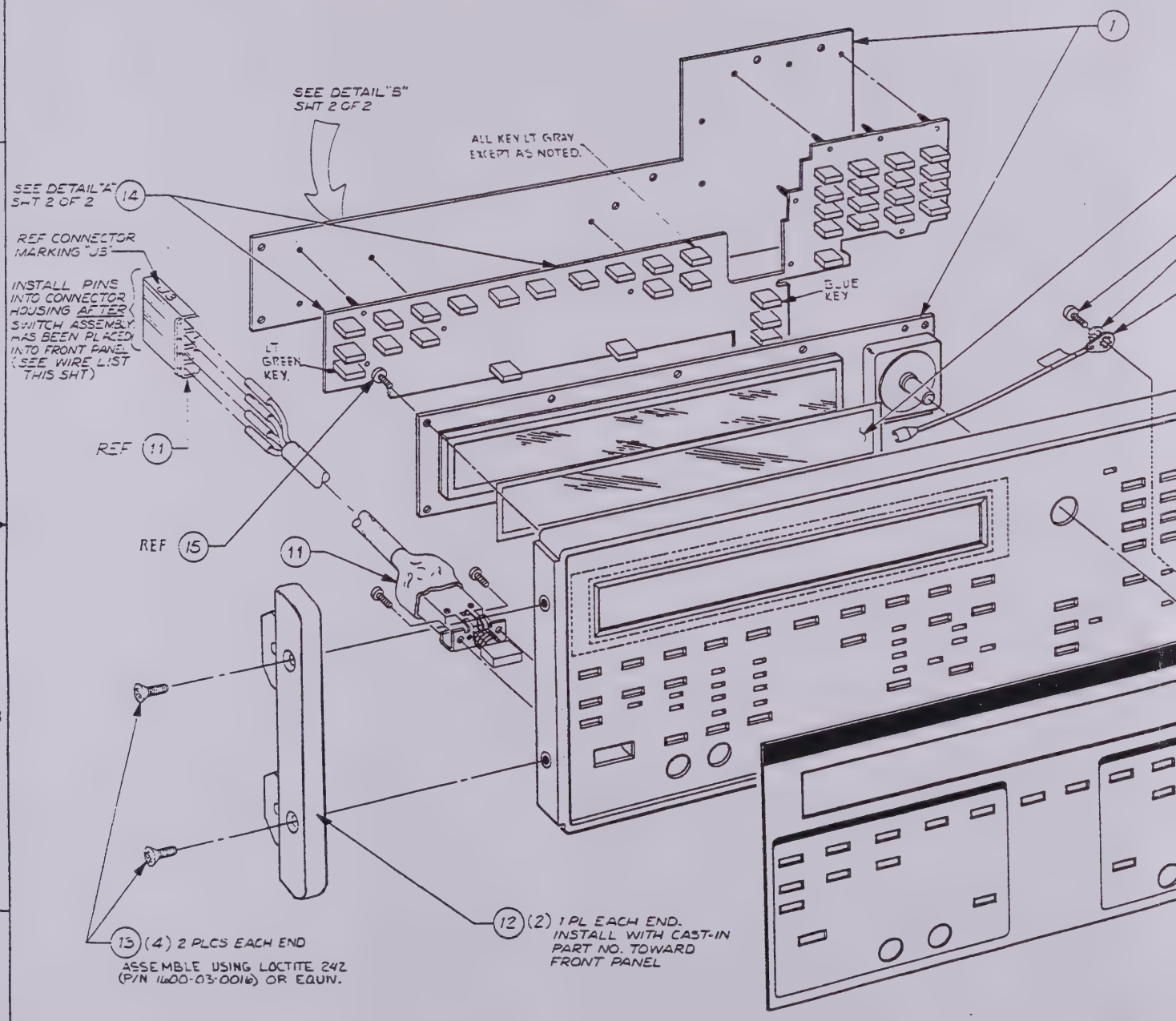
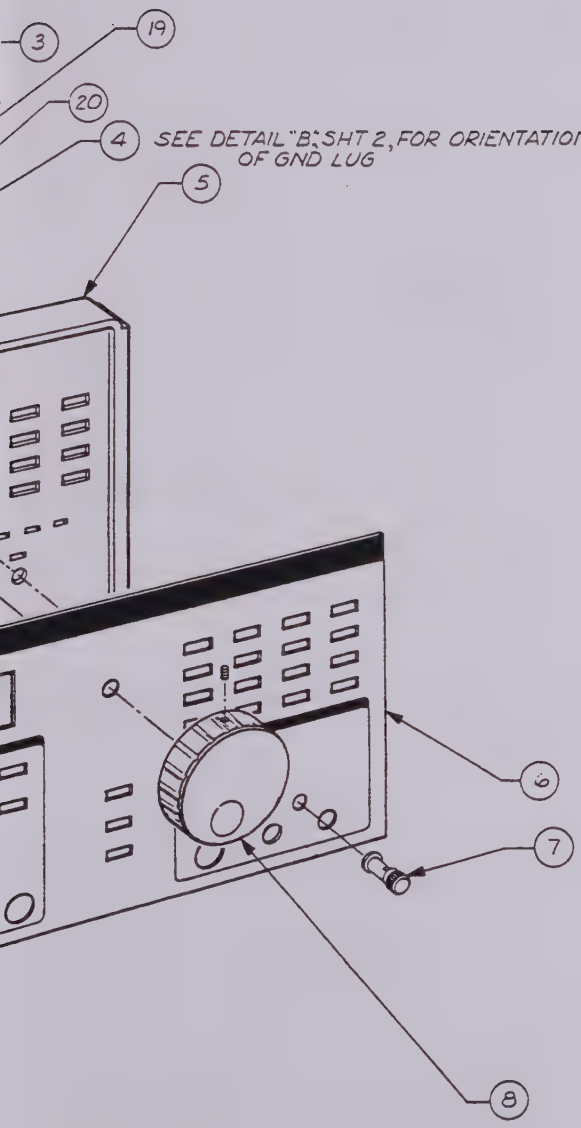

SEE DETAIL "B" SHT 2 OF 2
ALL KEY LT GRAY EXCEPT AS NOTED.
1
SEE DETAIL "A" SHT 2 OF 2
14
REF CONNECTOR MARKING "J3"
INSTALL PINS INTO CONNECTOR HOUSING AFTER SWITCH ASSEMBLY HAS BEEN PLACED INTO FRONT PANEL (SEE WIRE LIST THIS SHT)
J3
BLUE KEY
LT GREEN KEY.
REF 11
REF 15
11
13 (4) 2 PLCS EACH END
ASSEMBLE USING LOCTITE 242 (P/N 1600-03-00016) OR EQUIV.
12 (2) 1 PL EACH END. INSTALL WITH CAST-IN PART NO. TOWARD FRONT PANEL

1. MARK ASSEMBLY NO. "1101-00-3121 ", LATEST REV, MANUFACTURERS ID, FSCM 28338, PER MIL-STD-130, APPROX WHERE SHOWN.

NOTE UNLESS OTHERWISE SPECIFIED

| REV | ECO | BY | DATE | APP |
|---|---|---|---|---|
| A | ERC NO. 90-[illegible] | AD | | |
| [illegible] | ECO# 91-[illegible] | MS | [illegible] | |
| [illegible] | [illegible] | [illegible] | [illegible] | |




WIRE LIST

| "J3" CONN PIN NO. | WIRE COLOR | SWITCH TERMINAL (REF) |
|---|---|---|
| 3 | RED | 2A |
| 2 | WHT | 1A |
| 4 | GRN | 5B |
| 1 | BLK | 4B |

SEE SEPARATE PARTS LIST

| | | |
|---|---|---|
| REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN SC/AD | DATE 5 18 90 |
| MATERIAL # | CHECKED D. Bozell | 6/5/90 |
| | PROJ. ENGR. | 6/5/90 |
| | QA LEADS APPROV. | 6/6/90 |
| FINISH WAVETEK PROCESS # | UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ± / XX ± XXX ± / ± | |
| DO NOT SCALE DRAWING | | |

WAVETEK San Diego, California

TITLE: ASSEMBLY, FRONT PANEL

| SIZE | FSCM NO. | DWG. NO. | REV |
|---|---|---|---|
| D | 23338 | 1101-00-3321 | C |

SCALE NONE | MODEL 90 | SHEET 1 OF 2

1101-00-3321

D C B A

4 3 2 1

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D

C

B

A

NOTE UNLESS OTHERWISE SPECIFIED

8 7 6 5

| REV | ECO | BY | DATE | APP |
|---|---|---|---|---|

| REFERENCE DESIGNATORS | PART DESCRIPTION | ORIG-MFGR-PART-NO | MFGR | WAVETEK NO. | QTY/PT |
|---|---|---|---|---|---|
| 1 | PCA, DISPLAY/ KEYBOARD | 1100-00-3322 | WVTK | 1100-00-3322 | 1 |
| NONE | A/D FRONT PANEL ASSY | 1101-00-3321 | WVTK | 1101-00-3321 | 1 |
| 8 | ENCODER KNOB ASSY REF: A/D 1201-00-3380 | 1200-00-3380 | WVTK | 1200-00-3380 | 1 |
| 11 | CABLE ASSY, AC SWITCH AND CABLE | 1200-00-3391 | WVTK | 1200-00-3391 | 1 |
| 4 | WIRE ASSY | 1207-00-3010 | WVTK | 1207-00-3010 | 1 |
| 14 | KEYPAD, MODEL 90 | 1400-02-3240-01 | WVTK | 1400-02-3420-01 | 1 |
| 6 | OVERLAY FRONT PANEL MODEL 90 | 1400-02-3032 | WVTK | 1400-02-3032 | 1 |
| 12 | CORNER BRACKET, PAINTED | 1400-02-3034 | WVTK | 1400-02-3034 | 2 |
| 3 | WINDOW, DISPLAY | 1400-02-3073 | WVTK | 1400-02-3073 | 1 |
| 5 | FRONT PANEL MOLDED | 1400-02-3087 | WVTK | 1400-02-3087 | 1 |
| 7 | LUG, GROUNDING | 139 | SMITH | 2100-04-0043 | 1 |
| 20 | WASHER, LOCK, REG S/S #4 | MS 35338-136 | CMRCL | 2800-45-6000 | 1 |
| 13 | SCREW, 8-32 X 1/2, 100 DEG, FH, PHLPS, SS | 2800-54-8108 | CMCRL | 2800-54-8108 | 4 |

| WAVETEK PARTS LIST | TITLE FRONT PANEL ASSY | ASSEMBLY NO. 1100-00-3321 PAGE 1 | REV C |
|---|---|---|---|

| REFERENCE DESIGNATORS | PART DESCRIPTION | ORIG-MFGR-PART-NO | MFGR | WAVETEK NO. | QTY/PT |
|---|---|---|---|---|---|
| 15 | SCREW, 2 X 5/16, TYPE B, THD FORM, PH, SS | 2800-57-2905 | CMRCL | 2800-57-2905 | 23 |
| 19 | SCREW, PH, 6-32 X 5/16, PHLPS, NYLOK, SS | 2800-59-6105 | CMRCL | 2800-59-6105 | 1 |

| WAVETEK PARTS LIST | TITLE FRONT PANEL ASSY | ASSEMBLY NO. 1100-00-3321 PAGE 2 | REV C |
|---|---|---|---|

| REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN | DATE | WAVETEK SAN DIEGO, CALIFORNIA |
|---|---|---|---|
| MATERIAL | CHECKED | | TITLE PARTS LIST FRONT PANEL |
| | PROJ ENGR | | |
| FINISH WAVETEK PROCESS | RELEASE APPROV | | SIZE D FSCM NO. 23338 DWG. NO. 1100-00-3321 REV C |
| DO NOT SCALE DRAWING | UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ± .XX ± .XXX ± | | SCALE MODEL 90 SHEET 1 OF 1 |

4 3 2 1

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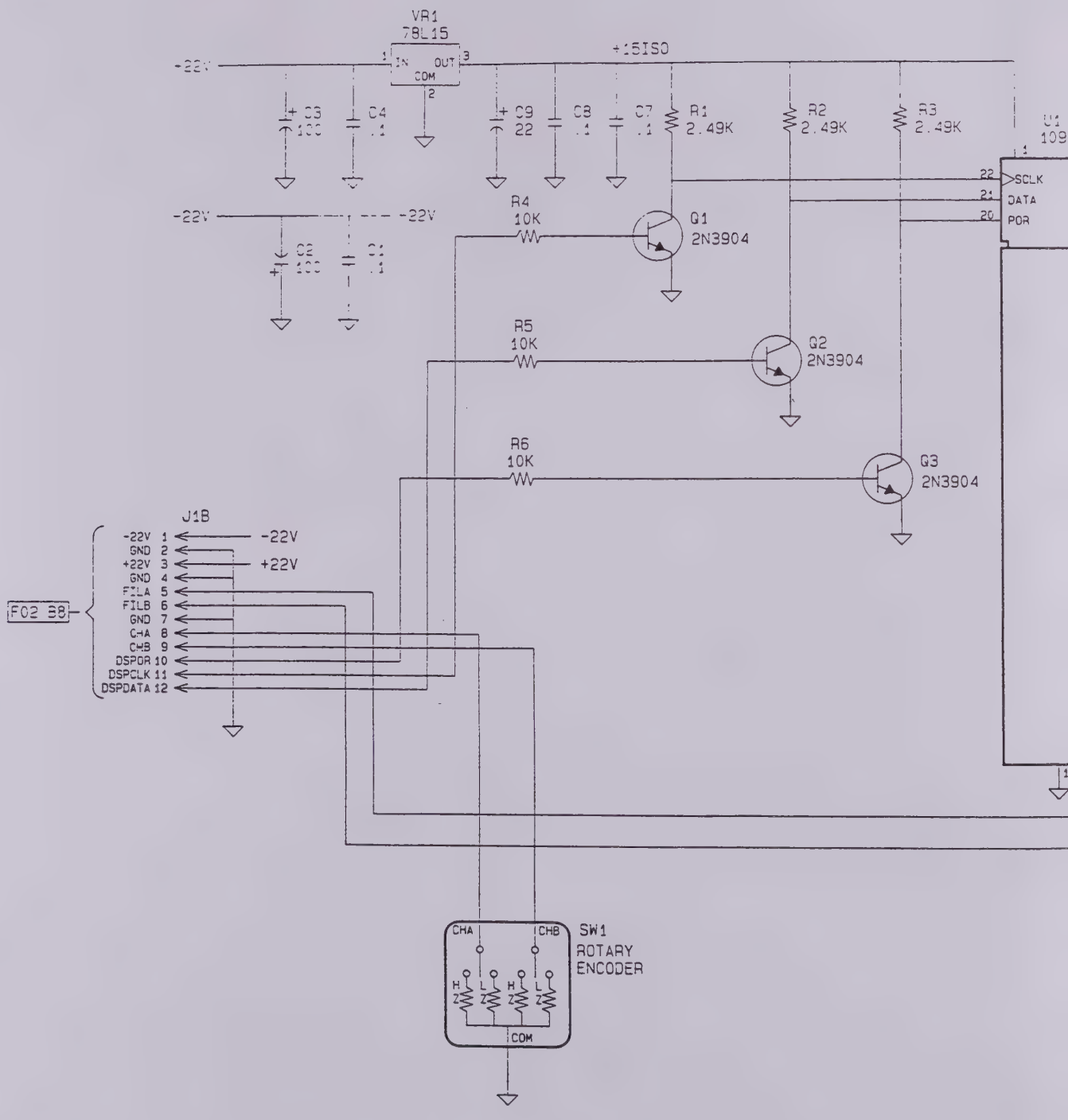



4. THESE PARTS ARE NOT INSTALLED.

3. FOR INSTRUMENT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC.

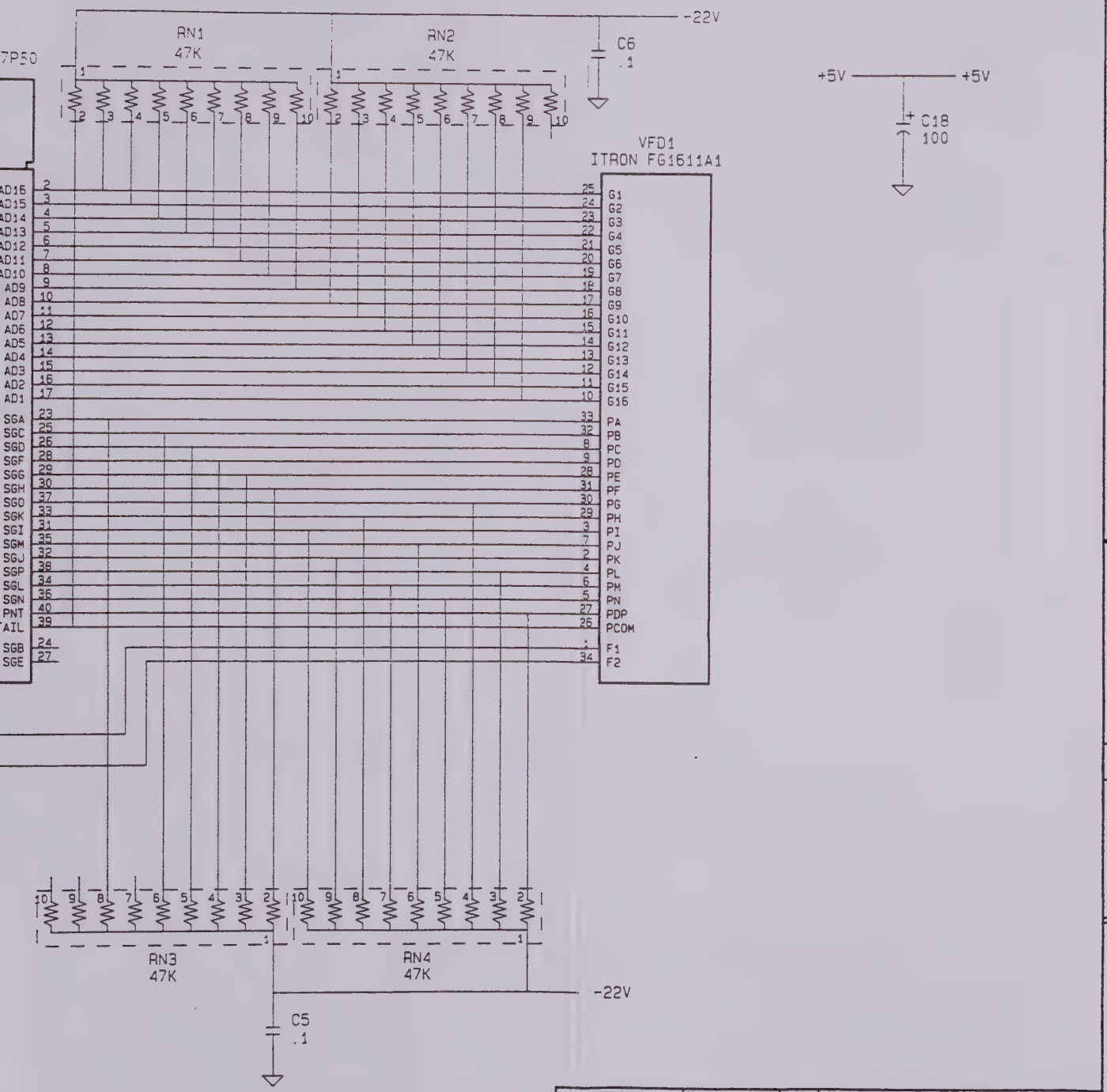
2. ALL CAPACITORS ARE IN MICROFARADS (uF).

1. ALL RESISTORS ARE IN OHMS, 1/8W, 1%, MF.

NOTE UNLESS OTHERWISE SPECIFIED

| REV | ECO | BY | DATE | APP |
|---|---|---|---|---|
| B | ECO 93-047 | [illegible] | [illegible] | [illegible] |
| C | ECO# 93-144 | MP | [illegible] | [illegible] |

# DISPLAY BOARD




| | | | |
|---|---|---|---|
| REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN A. TALMADGE | DATE 7-11-90 | WAVETEK SAN DIEGO, CALIFORNIA |
| MATERIAL | CHECKED | | TITLE |
| | PROJ. ENGR. | | SCHEMATIC, DISPLAY/KEYBOARD |
| FINISH WAVETEK PROCESS | RELEASE APPROV. | | |
| DO NOT SCALE DRAWING | UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES XX ± XXX ± | | SIZE D · FSCM NO. 23338 · DWG. NO. 1104-00-3322 · REV C · SCALE NONE · MODEL 90 SERIES · SHEET 1 OF 4 |

1104-00-3341

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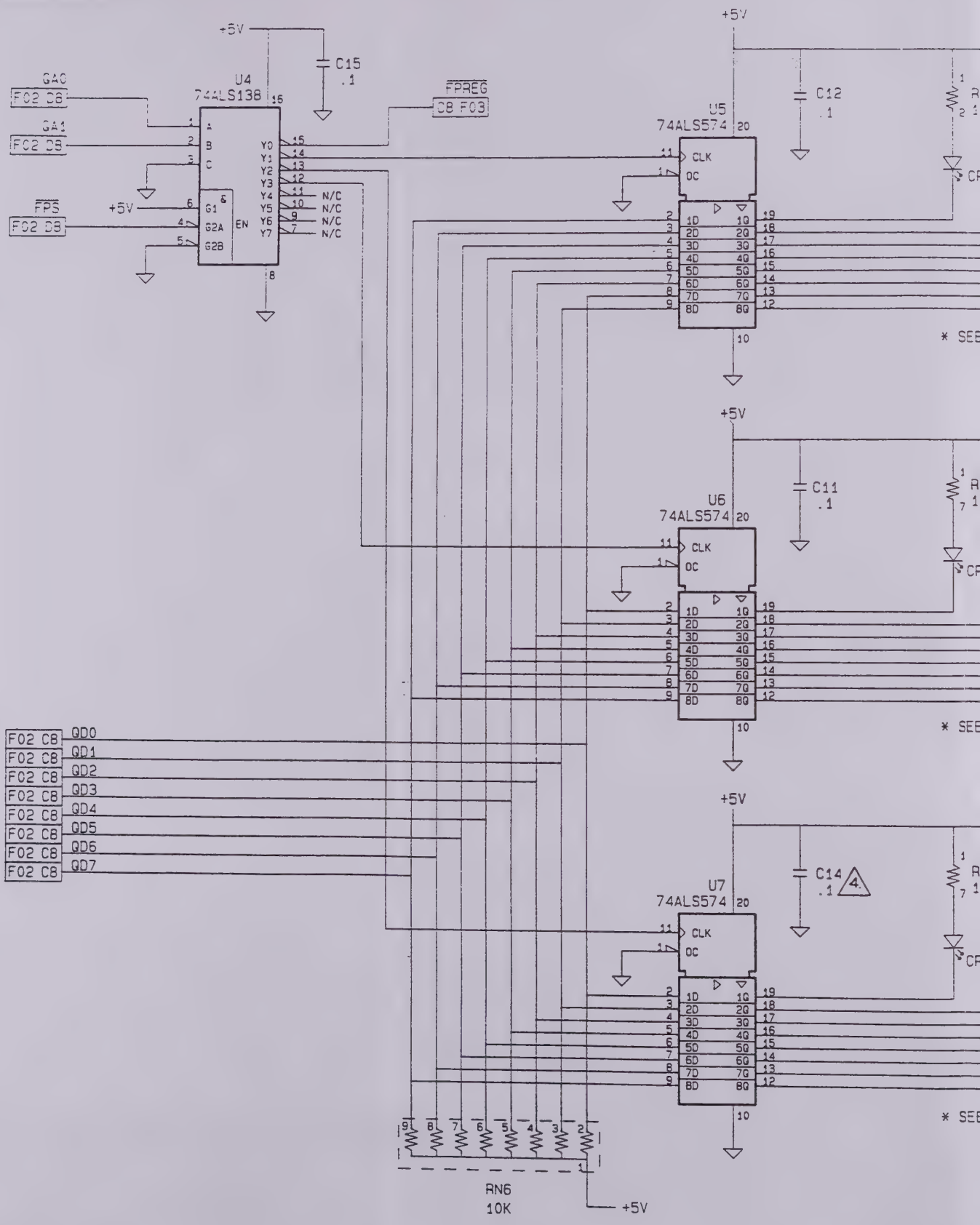
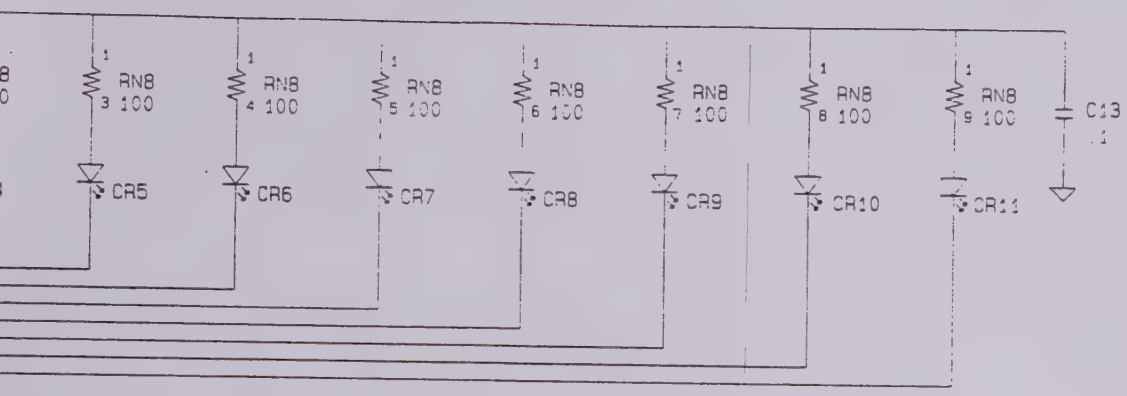
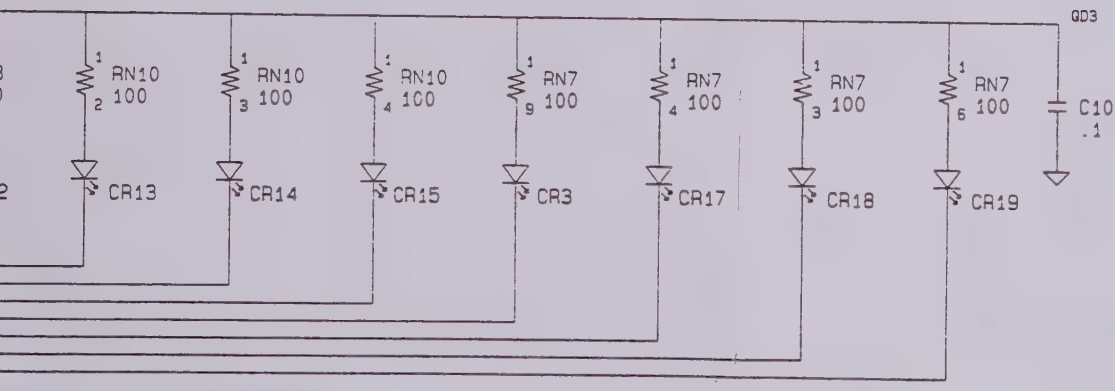


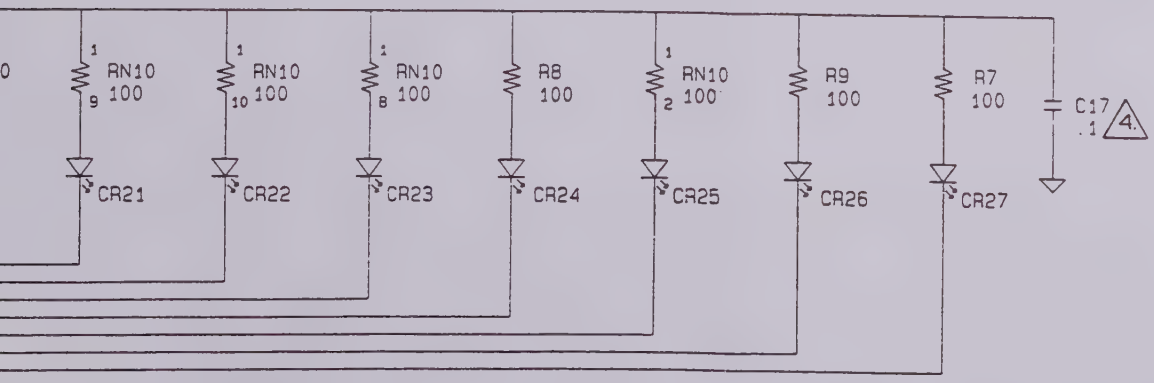

NOTE UNLESS OTHERWISE SPECIFIED




SHEET 4 FOR LED ASSIGNMENTS




SHEET 4 FOR LED ASSIGNMENTS




SHEET 4 FOR LED ASSIGNMENTS

| | | | |
|---|---|---|---|
| REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN A. TALMADGE | DATE 7-11-90 | WAVETEK San Diego, California |
| MATERIAL | CHECKED | 7-26-90 | TITLE: SCHEMATIC, DISPLAY/KEYBOARD |
| | PROJ. ENGR | 7/24/90 | |
| FINISH WAVETEK PROCESS | RELEASE APPROV. | 7/24/90 | |
| DO NOT SCALE DRAWING | UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ± XX ± .XXX ± | | SIZE D · FSCM NO. 23338 · DWG. NO. 1104-00-3322 · REV C · SCALE NONE · MODEL 90 SERIES · SHEET 3 OF 4 |

1104-00-3322 C

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NOTES:

1. COMPONENTS MOUNTED ON COMPONENT SIDE OF PCB SHOWN ON SHEET 1, COMPONENTS MOUNTED ON SOLDER SIDE OF PCB SHOWN ON SHEET 2.

2 RIBBON CABLE IS INSTALLED BETWEEN J1A ON LOWER KEYBOARD PCB AND J1B ON UPPER DISPLAY PCB.

3 LEADS OF COMPONENTS MOUNTED ON COMPONENT SIDE OF PCB OPPOSITE DISPLAY (VFD1), MUST HAVE LEADS TRIMMED TO WITHIN .050 OF PCB SURFACE.

4 MOUNTING OF DISPL

A. INSTALL AND SO

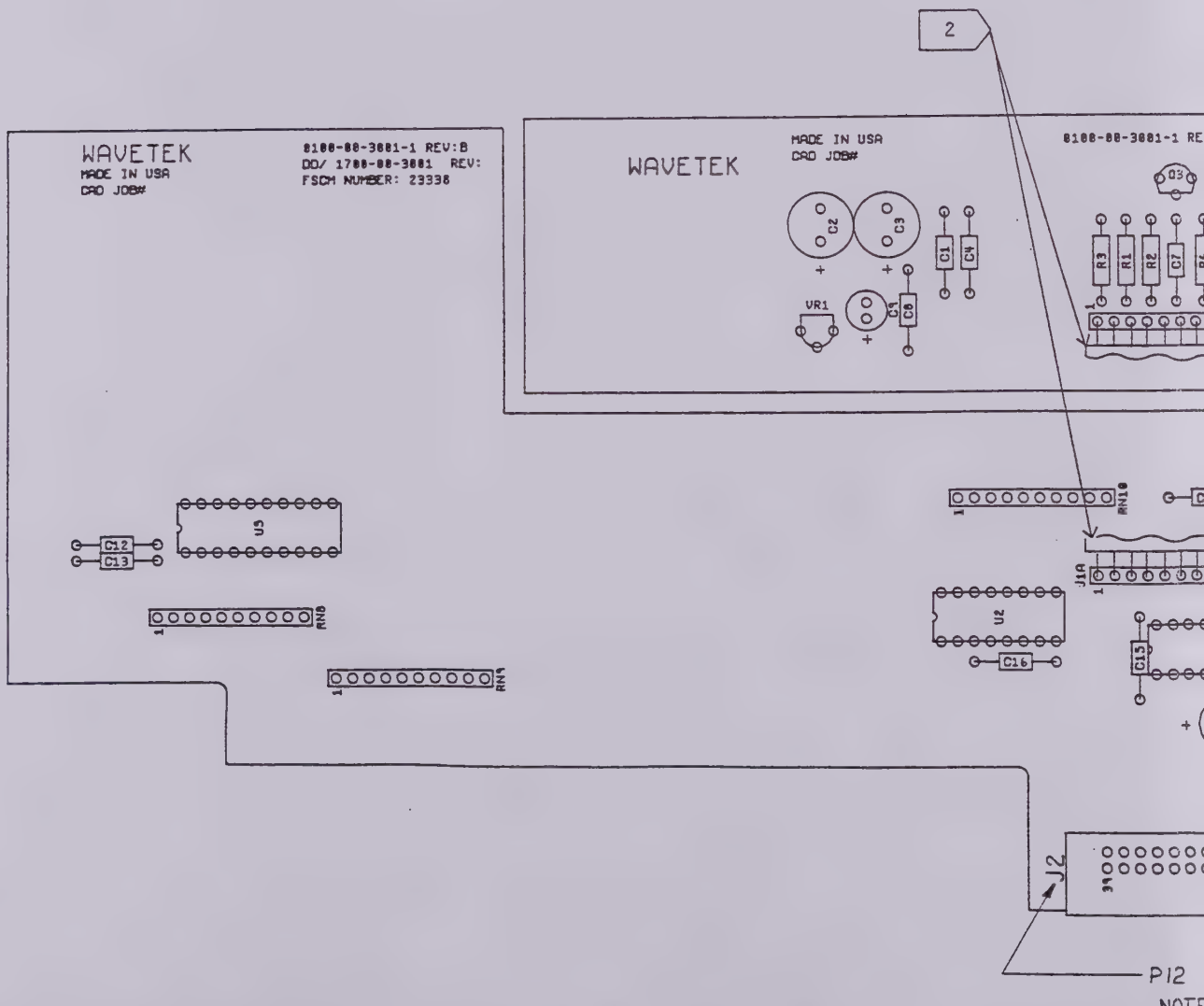
B. TRIM LEADS OF

C. ATTACH DISPLAY POSITIONING CU

D. PLACE DISPLAY SIDE OF PCB MA IS FLUSH TO TH PINS OF COMPO PIERCE THE CU

E. ALLOW DISPLAY BEFORE SOLDER

5 LEDS (CR1 THRU CR




COMPONENT SIDE

NOTE UNLESS OTHERWISE SPECIFIED

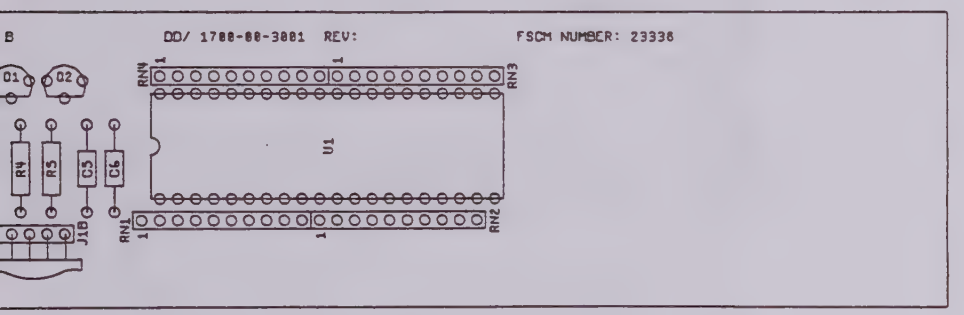
| REV | ECN | BY | DATE | APP |
|---|---|---|---|---|
| A | ERO [illegible] | | | |
| B | ECO [illegible] | SC | [illegible] | |

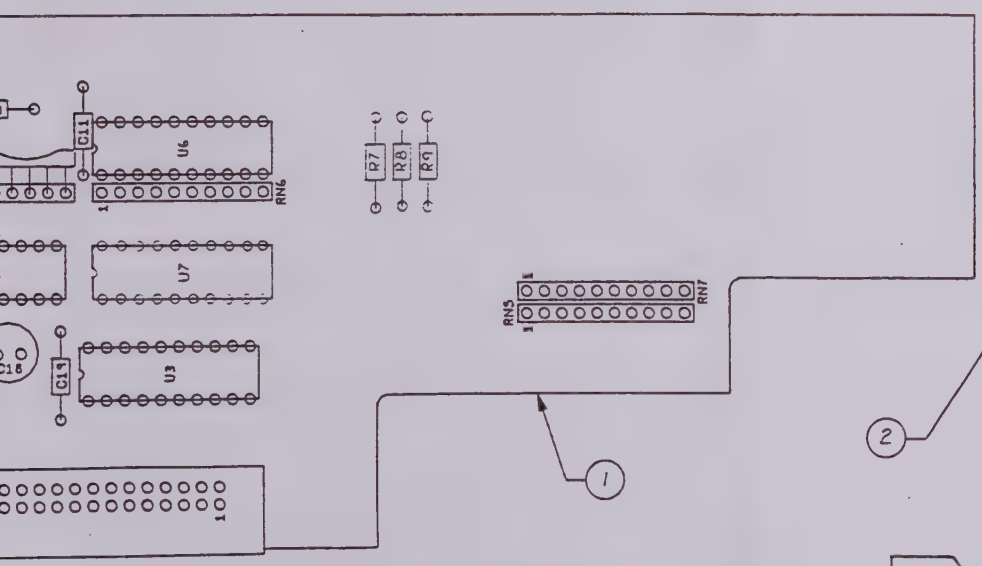
Y (VFD1):

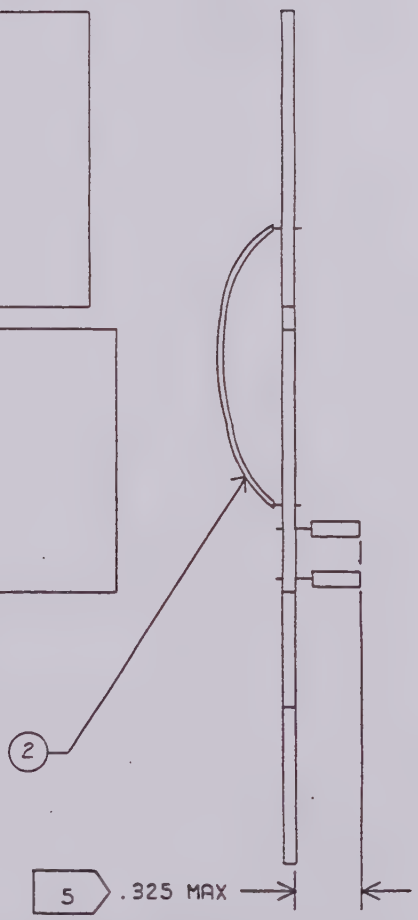
LDER COMPONENTS ON COMPONENT SIDE OF PCB.
COMPONENT ON UPPER BOARD PER NOTE 3.
CUSHION (ITEM NO.3) TO DISPLAY,
SHION SO THAT IT DOES NOT OVERLAP DISPLAY.
VFD1) WITH ATTACHED CUSHION ON SOLDER
KING SURE THAT THE SURFACE OF THE CUSHION
PCB SURFACE.
ENTS ON OPPOSITE SIDE OF PCB WILL
HION.

VFD1 ON COMPONENT SIDE) TO SELF-LEVEL
NG THE PINS OF DISPLAY.

7) MAY BE MOUNTED FLUSH TO PCB.




THIS CONNECTOR IS MARKED
J2 ON THE PC BOARD
SILKSCREEN

SEE SEPARATE PARTS LIST

| | | | |
|---|---|---|---|
| REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN A. TALMADGE | DATE 7-1-90 | WAVETEK SAN DIEGO, CALIFORNIA |
| MATERIAL | PROJ ENGR [illegible] | 7/1/90 | TITLE PCB ASSEMBLY - DISPLAY/KEYBOARD |
| FINISH WAVETEK PROCESS | RELEASE APPROV [illegible] | 7/1/90 | |
| | TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° XX ±.030 | | |
| | DO NOT SCALE DWG | MODEL NO 90 SERIES | DWG NO. 1101-00-3322 REV B |
| | SCALE NONE | CODE IDENT 23338 | SHEET 1 OF 2 |

1101-00-3322 B

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| REFERENCE DESIGNATORS | PART DESCRIPTION |
|---|---|
| REF | A/D. DISPLAY/ KEYBOARD |
| REF | S/D DISPLAY. KEYBOARD |
| 3 | CUSHION. DISPLAY |
| C1 C10 C11 C12 C13 C15 C16 C19 C4 C5 C6 C7 C8 | CAP. CER. MON. .1MF. 50V. AXIAL |
| C18 C2 C3 | CAP. ELECT. 100MF. 35V RADIAL LEAD. SP .20 |
| C9 | CAP. ELECT. 22MF. 25V. RA DIAL |
| 1 | PCB. DISPLAY/KEYBOARD REF. SPEC 0008-00-0455 REV E |
| P12 | CONN. HEADER. 40 PIN. PCB MT. .1 CTR. 2X20. SHRD |
| VFD1 | DISPLAY. VAC. FLOUR |
| R7 R8 R9 | RES. MF. 1/8W. 1%. 100 |
| R4 R5 R6 | RES. MF. 1/8W. 1%. 10K |
| R1 R2 R3 | RES. MF. 1/8W. 1%. 2. 49K |
| RN5 RN6 RN9 | RES NETWORK 10K 2% |

WAVETEK PARTS LIST

TITLE
PCA. DISPLAY/ KEYBOARD

| REFERENCE DESIGNATORS | PART DESCRIPTION |
|---|---|
| | 10PIN SIP BUSS |
| RN1 RN2 RN3 RN4 | RES NETWORK 47K 2% 10PIN SIP BUSS |
| RN10 RN7 RN8 | RES NETWORK 10PIN SIP 100 OHM BUSS |
| CR1 CR10 CR11 CR7 CR9 | LED. AMBER. RECT BAR |
| CR12 CR13 CR14 CR15 CR17 CR18 CR19 CR2 CR20 CR21 CR22 CR23 CR24 CR25 CR26 CR27 CR3 CR4 CR5 CR6 CR8 | LED. GREEN. RECT BAR |
| Q1 Q2 Q3 | TRANS 2N3904 NPN GENERAL PURPOSE TO-92 |
| SW1 | ENCODER. ROTARY. MADE FROM 3104-00-0027 |
| 2 | CABLE. FLEX. JMP. ASSY |
| VR1 | VOLT REGULATOR. POSITIVE |
| U2 | MUX/DEMUX. ANALOG |
| U1 | CONTROLLER. ALPH NUM DISP. 40V |
| U4 | DECODER/DEMUX. 3 TO 8 LINE |

WAVETEK PARTS LIST

TITLE
PCA. DISPLAY/ KEYBOARD

NOTE UNLESS OTHERWISE SPECIFIED

| REV | ECO | BY | DATE | APP'D |
|---|---|---|---|---|

| ORIG-MFGR-PART-NO | MFGR | WAVETEK NO | QTY/PT |
|---|---|---|---|
| 1101-00-3322 | WVTK | 1101-00-3322 | 1 |
| 1104-00-3322 | WVTK | 1104-00-3322 | 1 |
| 1400-02-3510 | WVTK | 1400-02-3510 | 1 |
| CAC03Z5U104Z050A | CORNG | 1500-01-0405 | 13 |
| NRE101M35V10X12.5(OBS) | NIC | 1500-31-0102 | 3 |
| SRA25V822RM6X7LL | UNCON | 1500-32-2002 | 1 |
| 1700-00-3001 | WVTK | 1700-00-3001 | 1 |
| 1-102692-3 | AMP | 2100-02-0258 | 1 |
| FIP16A11R | NEC | 2400-03-0019 | 1 |
| RN55D-1000F | TRW | 4701-03-1000 | 3 |
| RN55D-1002F | TRW | 4701-03-1002 | 3 |
| RN55D-2491F | TRW | 4701-03-2491 | 3 |
| 4310R-101-103 | BOURN | 4770-00-0008 | 3 |

| ASSEMBLY NO. 1100-00-3322 | REV D |
|---|---|
| PAGE 1 | |

| ORIG-MFGR-PART-NO | MFGR | WAVETEK NO. | QTY/PT |
|---|---|---|---|
| 4310R-101-473 | BOURN | 4770-00-0030 | 4 |
| 4310R-101-101 | BOURN | 4770-00-0054 | 3 |
| LTL-3251A | LITE | 4899-00-0056 | 5 |
| LTL-3231A | LITE | 4899-00-0057 | 21 |
| 2N3904 | FAIR | 4901-03-9040 | 3 |
| 5109-00-0001 | WVTK | 5109-00-0001 | 1 |
| 1-86943-1 | AMP | 6001-60-0017 | 1 |
| 78L15 | TI | 7000-78-1501 | 1 |
| CD4051BE | RCA | 8000-40-5100 | 1 |
| 10957P-50 | ROCK | 8001-09-5700 | 1 |
| SN74ALS138N | TI | 8007-41-3800 | 1 |

| ASSEMBLY NO. 1100-00-3322 | REV D |
|---|---|
| PAGE 2 | |

| REFERENCE DESIGNATORS | PART DESCRIPTION | ORIG-MFGR-PART-NO | MFGR | WAVETEK NO | QTY/PT |
|---|---|---|---|---|---|
| U3 U5 U6 U7 | FLIP-FLOP, OCTAL D | SN74ALS574N | TI | 8007-45-7450 | 4 |

| WAVETEK PARTS LIST | TITLE PCA, DISPLAY/ KEYBOARD | ASSEMBLY NO. 1100-00-3322 | REV D |
|---|---|---|---|
| | | PAGE 3 | |

| | | | |
|---|---|---|---|
| REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN | DATE | WAVETEK SAN DIEGO, CALIFORNIA |
| MATERIAL | CHECKED | | TITLE |
| | PROJ. ENGR. | | PARTS LIST DISPLAY/KEYBOARD |
| | RELEASE APPROV. | | |
| FINISH WAVETEK PROCESS | UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ± .XX ± .XXX ± | | SIZE D / FSCM NO. 23338 / DWG. NO. 1100-00-3322 / REV D |
| DO NOT SCALE DRAWING | | | SCALE / MODEL 90 / SHEET 1 OF 1 |

4 3 2 1

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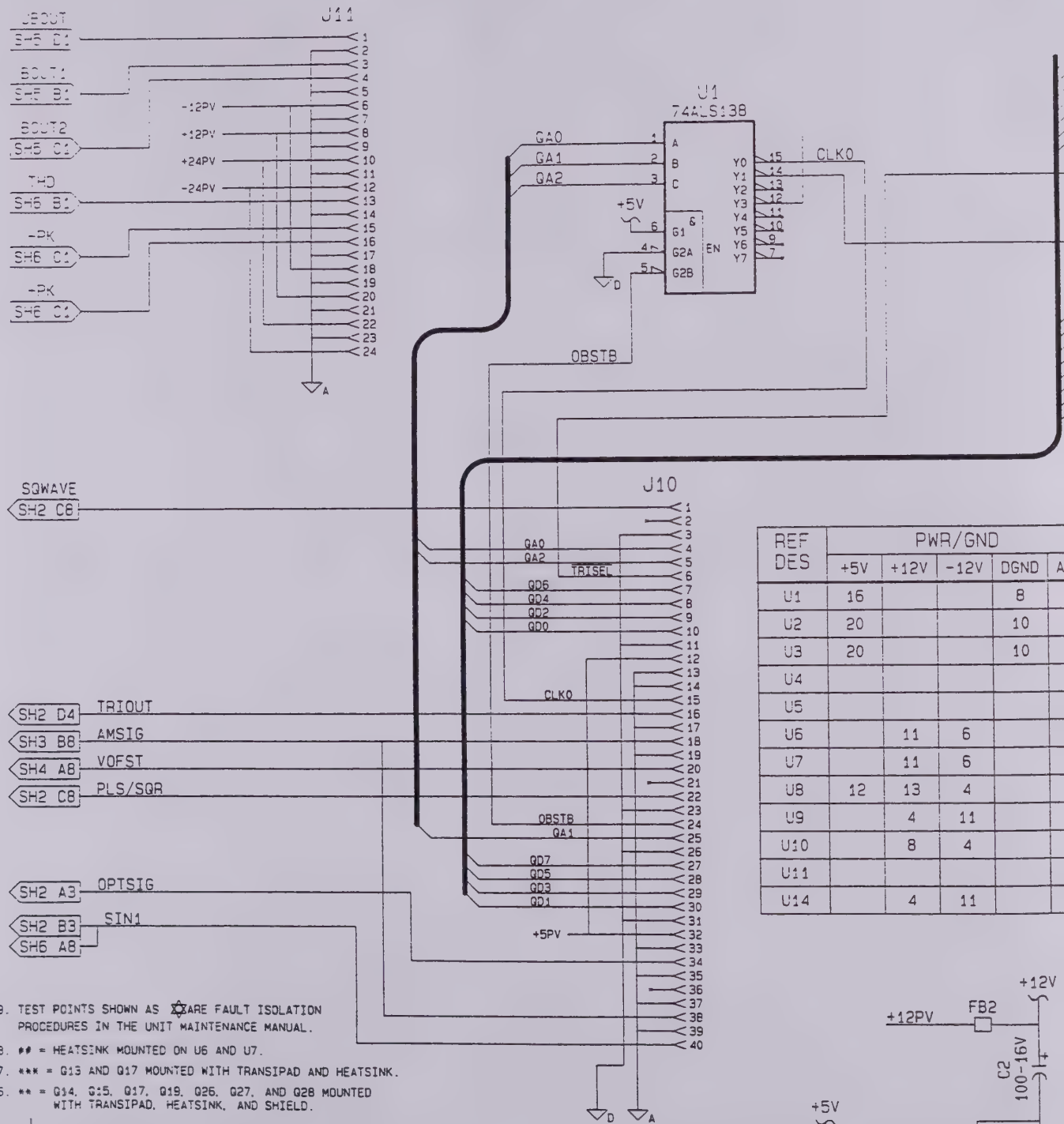
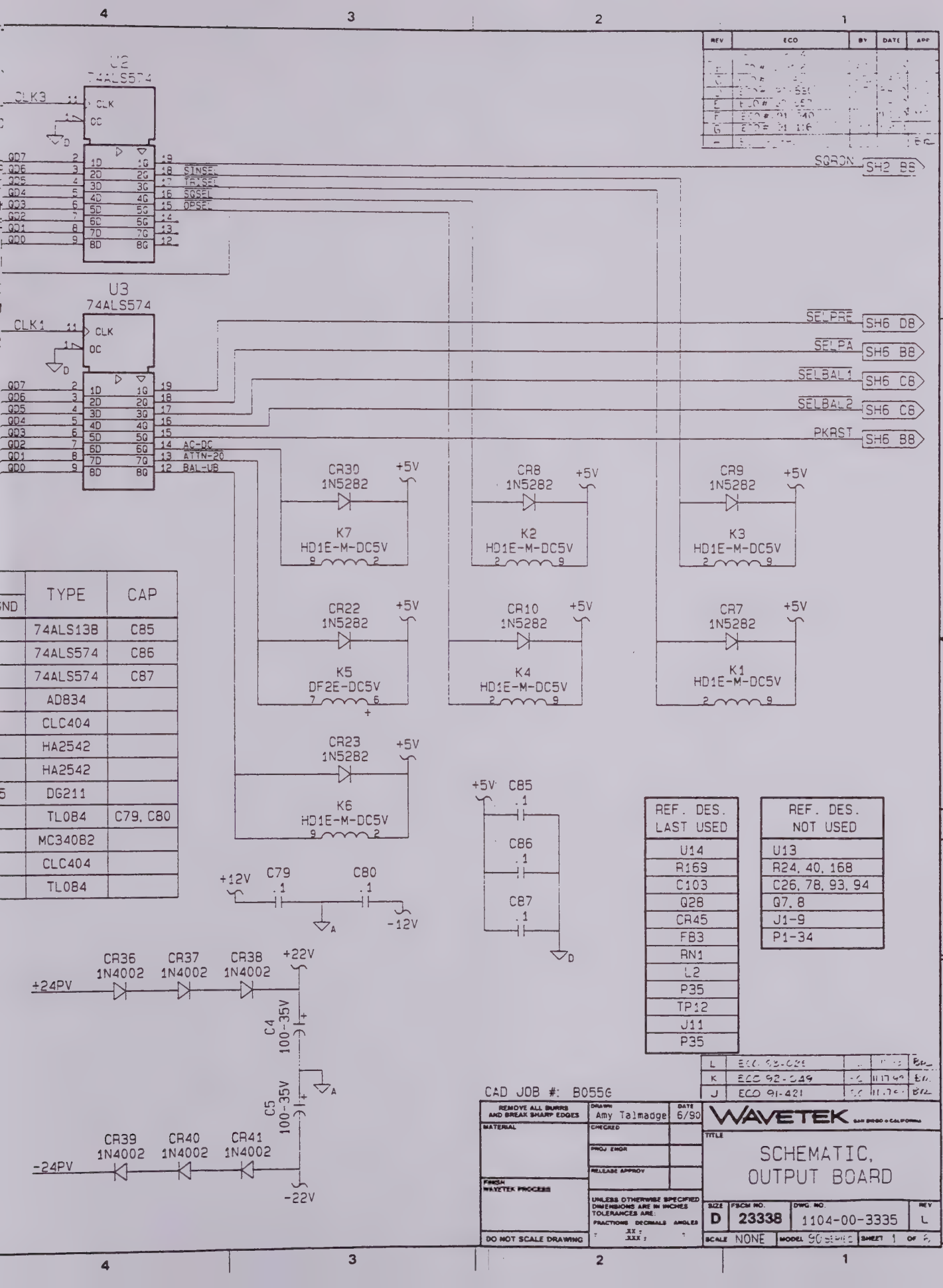



| REF DES | PWR/GND | | | | |
|---|---|---|---|---|---|
| | +5V | +12V | -12V | DGND | A |
| U1 | 16 | | | 8 | |
| U2 | 20 | | | 10 | |
| U3 | 20 | | | 10 | |
| U4 | | | | | |
| U5 | | | | | |
| U6 | | 11 | 6 | | |
| U7 | | 11 | 6 | | |
| U8 | 12 | 13 | 4 | | |
| U9 | | 4 | 11 | | |
| U10 | | 8 | 4 | | |
| U11 | | | | | |
| U14 | | 4 | 11 | | |

9. TEST POINTS SHOWN AS ✡ ARE FAULT ISOLATION PROCEDURES IN THE UNIT MAINTENANCE MANUAL.
8. ## = HEATSINK MOUNTED ON U6 AND U7.
7. *** = Q13 AND Q17 MOUNTED WITH TRANSIPAD AND HEATSINK.
6. ** = Q14, Q15, Q17, Q19, Q26, Q27, AND Q28 MOUNTED WITH TRANSIPAD, HEATSINK, AND SHIELD.
5. ⏚A IS THE ANALOG GROUND SYMBOL.
4. ⏚D IS THE DIGITAL GROUND SYMBOL.
3. ALL CAPACITORS ARE VALUED IN MICROFARADS (uF).
2. ALL RESISTORS ARE VALUED IN OHMS, 1/8W, 1%.
1. FOR INSTRUMENT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 1004-00-0596 FOR MODEL 90 AND 1004-00-0599 FOR MODEL 95.

NOTE UNLESS OTHERWISE SPECIFIED




| GND | TYPE | CAP |
|---|---|---|
| | 74ALS138 | C85 |
| | 74ALS574 | C86 |
| | 74ALS574 | C87 |
| | AD834 | |
| | CLC404 | |
| | HA2542 | |
| | HA2542 | |
| 5 | DG211 | |
| | TL084 | C79, C80 |
| | MC34082 | |
| | CLC404 | |
| | TL084 | |

| REF. DES. LAST USED |
|---|
| U14 |
| R169 |
| C103 |
| Q28 |
| CR45 |
| FB3 |
| RN1 |
| L2 |
| P35 |
| TP12 |
| J11 |
| P35 |

| REF. DES. NOT USED |
|---|
| U13 |
| R24, 40, 168 |
| C26, 78, 93, 94 |
| Q7, 8 |
| J1-9 |
| P1-34 |

| REV | ECO | BY | DATE | APP |
|---|---|---|---|---|
| L | ECO 92-029 | | | |
| K | ECO 92-049 | | 11/92 | |
| J | ECO 91-421 | | 11/91 | |

CAD JOB #: B0556

| | | |
|---|---|---|
| REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN Amy Talmadge | DATE 6/90 |
| MATERIAL | CHECKED | |
| | PROJ ENGR | |
| | RELEASE APPROV | |
| FINISH WAVETEK PROCESS | UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ; .XXX ; | |
| DO NOT SCALE DRAWING | | |

WAVETEK SAN DIEGO, CALIFORNIA

TITLE
SCHEMATIC,
OUTPUT BOARD

| SIZE | FSCM NO. | DWG. NO. | REV |
|---|---|---|---|
| D | 23338 | 1104-00-3335 | L |

SCALE NONE MODEL 9000 SERIES SHEET 1 OF 6

1104-00-3335 L

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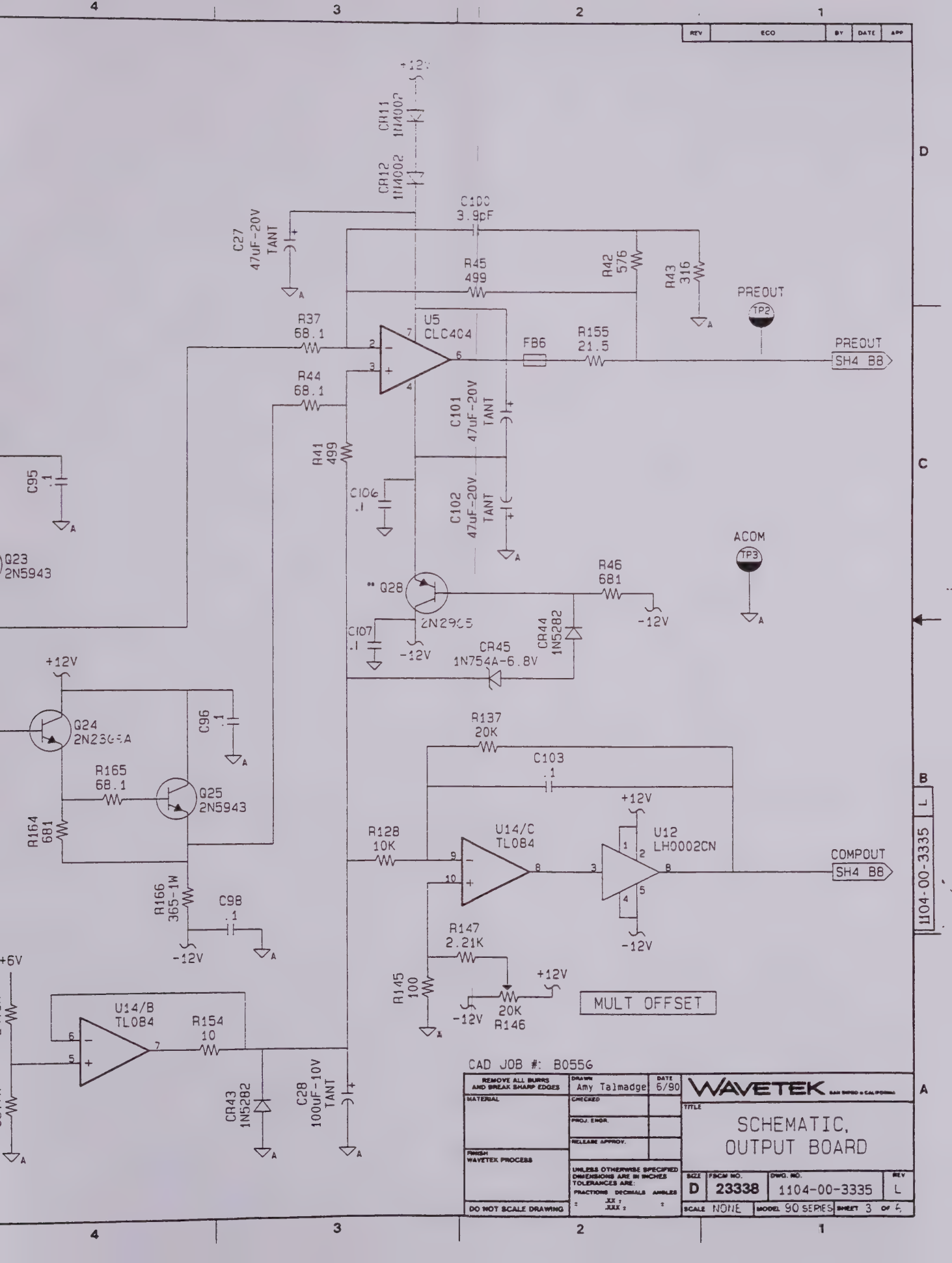
# PREAMPLIFIER AND MULTIPLIER

+12V
R142 46.4
Q26 " 2N2219A
+6V
TP11
C13 .1
C14 .1
C15 220-10V
R32 200
R34 100
R33 100
C23 .1
C29 10-25V
MULT FEED THRU
R25 2K
-6V
C20 .01
R159 33.2
Q22 2N2369A
R161 68.1
R160 681
R26 10K
PREAMPIN
SH2 D1
U4 AD834
+VS
Y1
Y2
X1
X2
-VS
W1
W2
R28 332
R175 301K
R27 1K
AMSIG
SH1 B8
R143 20K
C19 56pF
R30 499
R29 75
R31 332
R35 10
R36 10
C21 .01
-6V
TP12
R162 365-1W
C97 .1
-12V
U14/D TL084
Q27 " 2N2905
C17 .1
C18 220-10V
C22 .1
C30 10-25V
R144 10K
C16 .1
R148 46.4

NOTE UNLESS OTHERWISE SPECIFIED


REV ECO BY DATE APP
CR11 1N4002
CR12 1N4002
C100 3.9pF
C27 47uF-20V TANT
R45 499
R42 576
R43 316
PREOUT
TP2
R37 68.1
U5 CLC404
FB6
R155 21.5
PREOUT SH4 B8
R44 68.1
C101 47uF-20V TANT
R41 499
C95 .1
C106 .1
C102 47uF-20V TANT
ACOM
TP3
Q23 2N5943
Q28 2N2905
R46 681
-12V
C107 .1
CR45 1N754A-6.8V
CR44 1N5282
+12V
Q24 2N2369A
C96 .1
R165 68.1
Q25 2N5943
R164 681
R137 20K
C103 .1
R128 10K
U14/C TL084
U12 LH0002CN
COMPOUT SH4 B8
R166 365-1W
C98 .1
R147 2.21K
R145 100
20K R146
MULT OFFSET
+6V
U14/B TL084
R154 10
CR43 1N5282
C28 100uF-10V TANT
CAD JOB #: B055G
REMOVE ALL BURRS AND BREAK SHARP EDGES
DRAWN Amy Talmadge 6/90
CHECKED
PROJ. ENGR.
RELEASE APPROV.
MATERIAL
FINISH WAVETEK PROCESS
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES XX ± XXX ±
DO NOT SCALE DRAWING
WAVETEK SAN DIEGO, CALIFORNIA
TITLE
SCHEMATIC, OUTPUT BOARD
SIZE D FSCM NO. 23338 DWG. NO. 1104-00-3335 REV L
SCALE NONE MODEL 90 SERIES SHEET 3 OF 6
1104-00-3335 L

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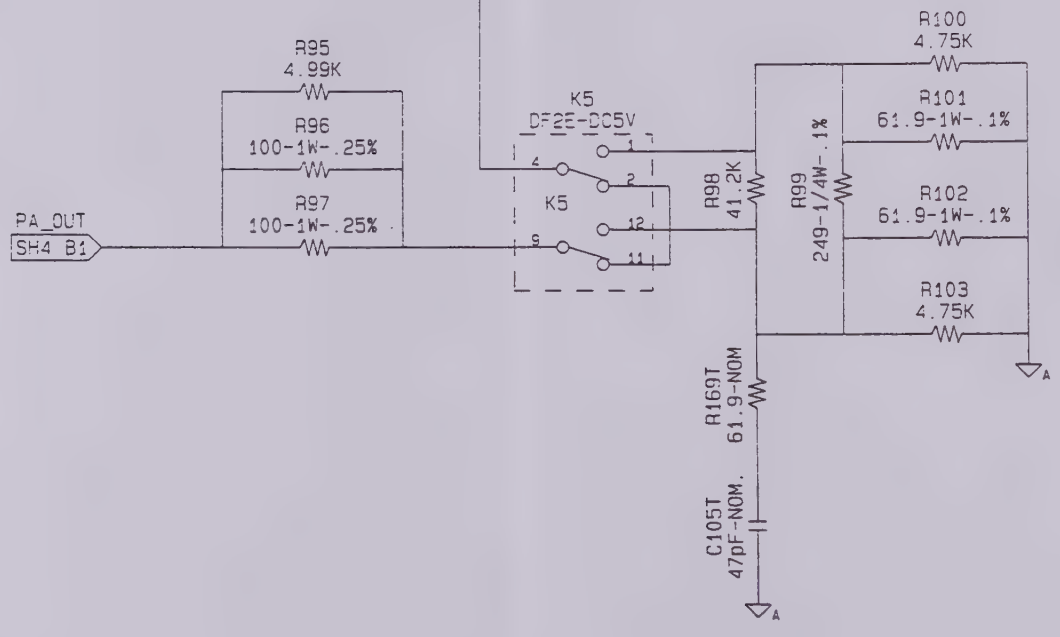
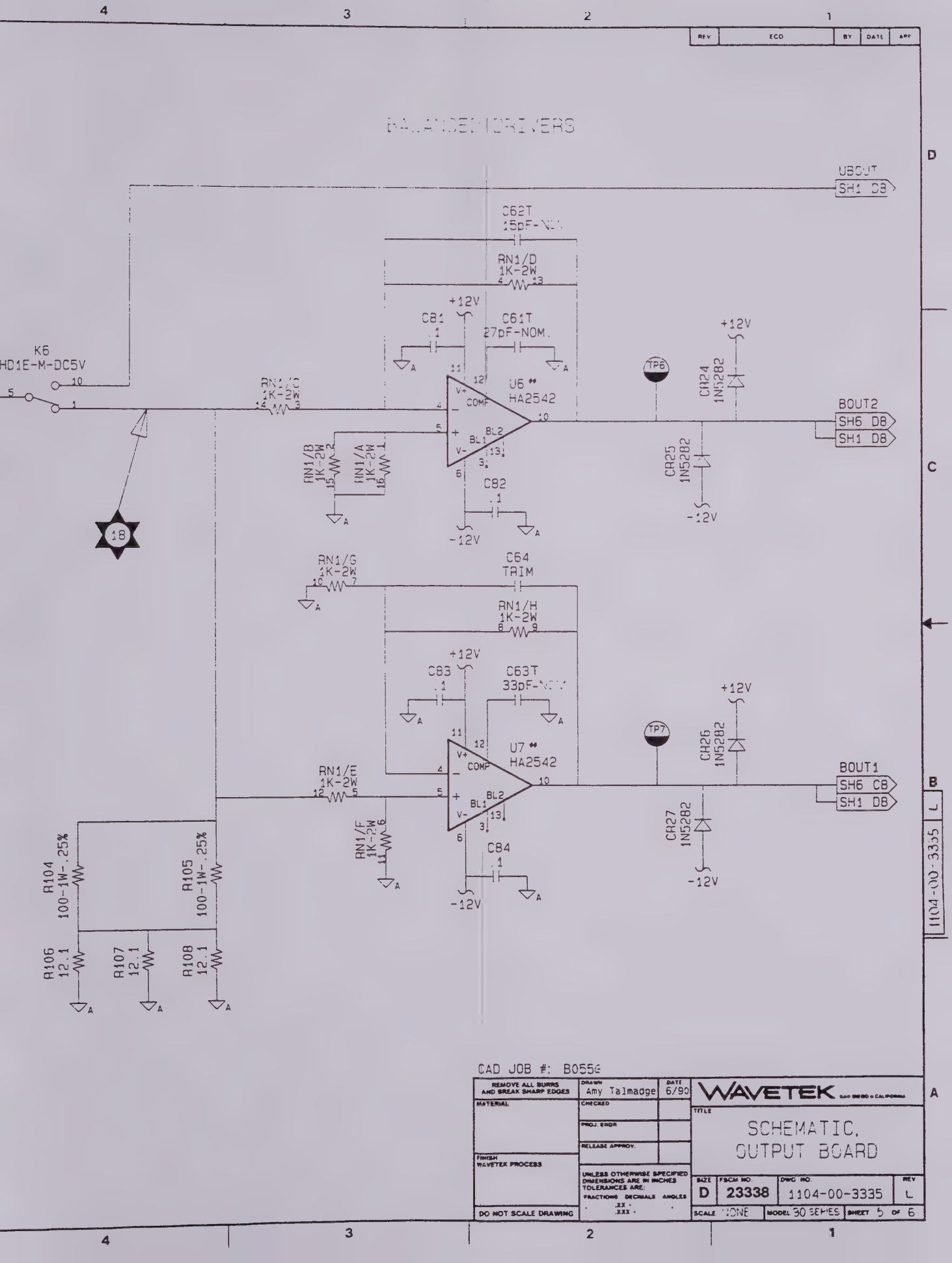
# -20dB ATTENUATOR




NOTE UNLESS OTHERWISE SPECIFIED


BALANCE DRIVERS
UBOUT
SH1 D8
C62T
15pF-NOM.
RN1/D
1K-2W
+12V
C81
.1
C61T
27pF-NOM.
K6
HD1E-M-DC5V
U6 **
HA2542
V+
COMP
BL2
BL1
V-
TP6
CR24
1N5282
BOUT2
SH6 D8
SH1 D8
RN1/B
1K-2W
RN1/A
1K-2W
C82
.1
-12V
CR25
1N5282
18
RN1/G
1K-2W
C64
TRIM
RN1/H
1K-2W
C83
.1
C63T
33pF-NOM.
U7 **
HA2542
TP7
CR26
1N5282
BOUT1
SH6 C8
SH1 D8
RN1/E
1K-2W
RN1/F
1K-2W
C84
.1
CR27
1N5282
R104
100-1W-.25%
R105
100-1W-.25%
R106
12.1
R107
12.1
R108
12.1
REV
ECO
BY
DATE
APP
1104-00-3335
L
CAD JOB #: B055G
REMOVE ALL BURRS AND BREAK SHARP EDGES
DRAWN
Amy Talmadge
DATE
6/90
CHECKED
PROJ. ENGR
RELEASE APPROV.
MATERIAL
FINISH
WAVETEK PROCESS
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.XX
.XXX
DO NOT SCALE DRAWING
WAVETEK
TITLE
SCHEMATIC,
OUTPUT BOARD
SIZE
D
FSCM NO.
23338
DWG NO.
1104-00-3335
REV
L
SCALE NONE
MODEL 30 SERIES
SHEET 5 OF 6

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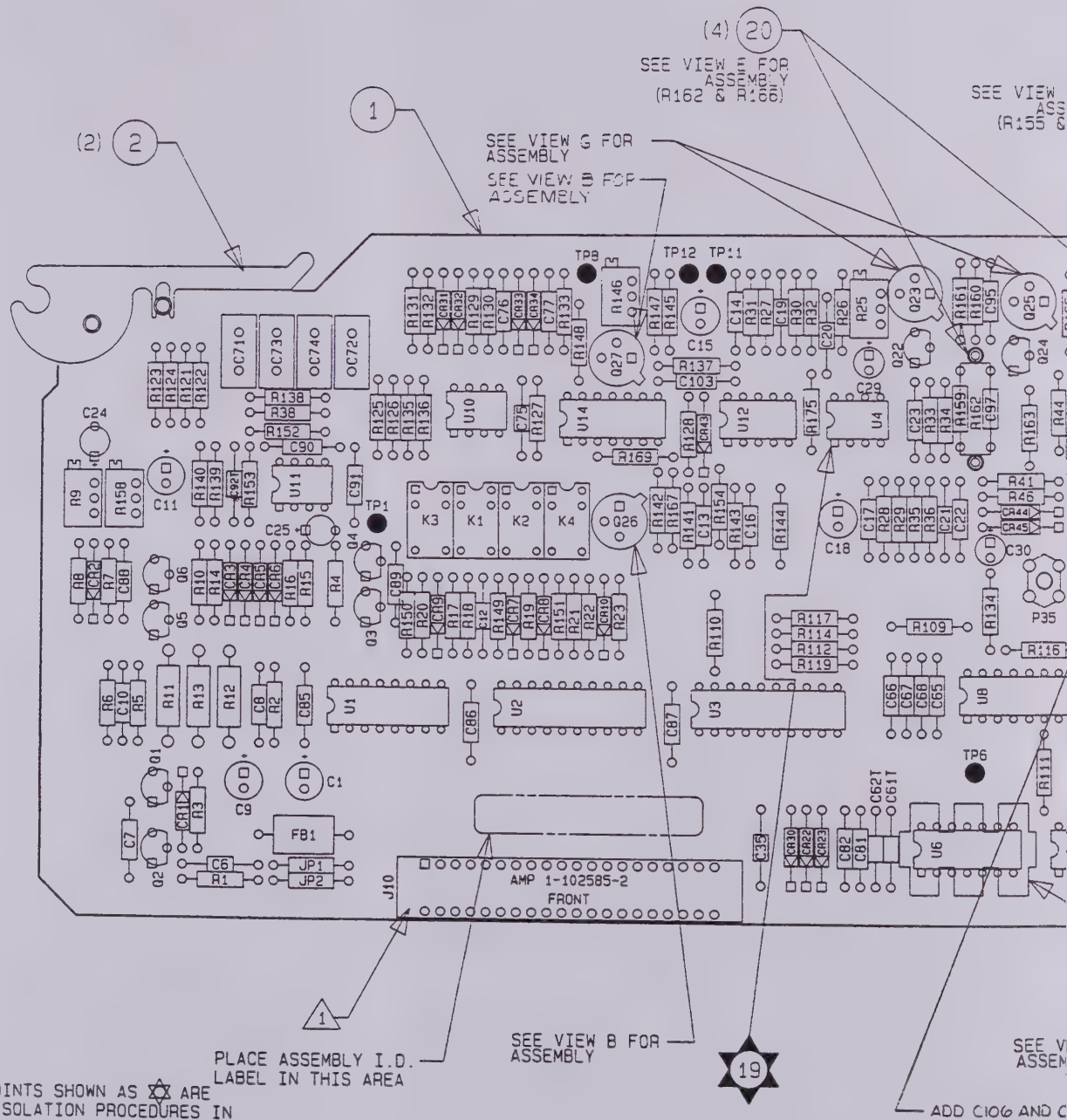


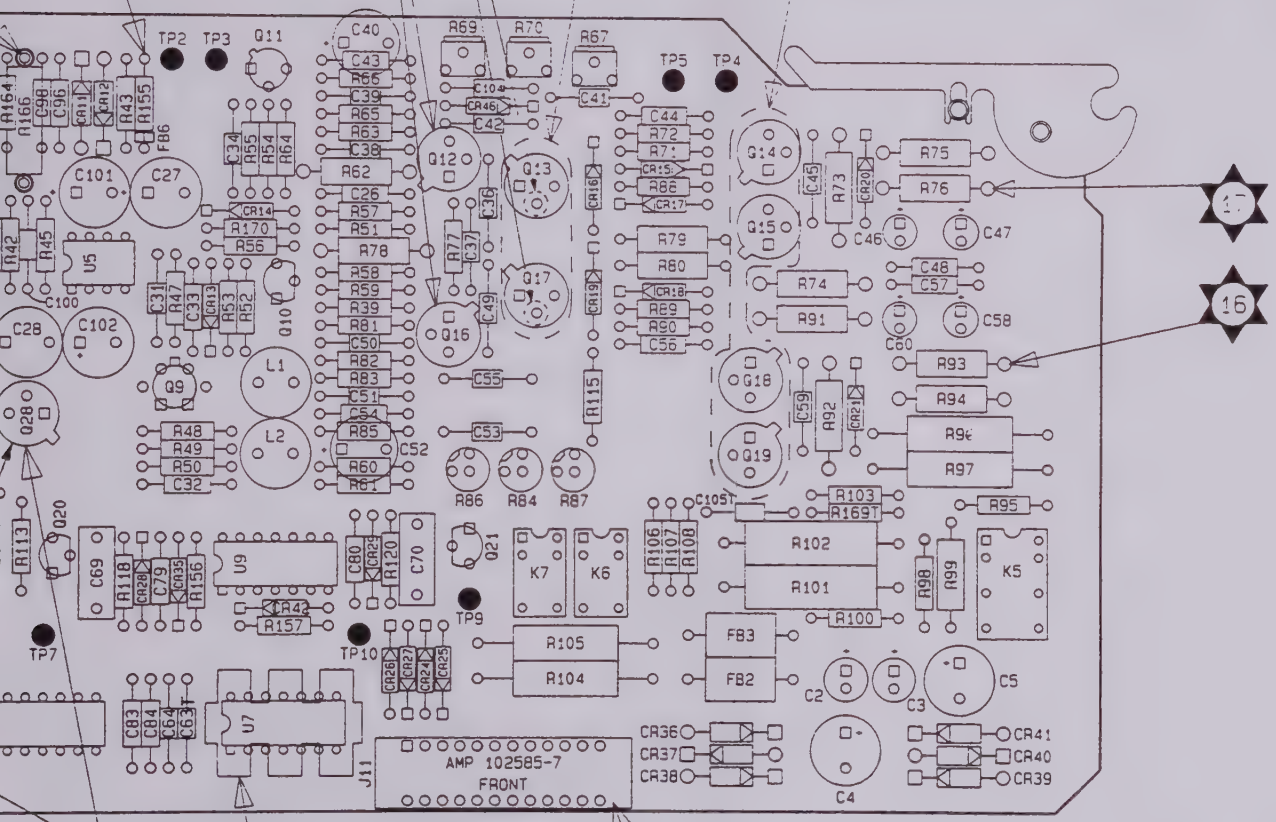

6. TEST POINTS SHOWN AS ✡ ARE FAULT ISOLATION PROCEDURES IN THE UNIT MAINTENANCE MANUAL.
5. ASSEMBLE PER WAVETEK WORKMANSHIP STANDARDS.
4. REFERENCE DESIGNATIONS DO NOT APPEAR ON PARTS.
3. FOR ASSEMBLY INTERCONNECTION, SEE INSTRUMENT SCHEMATIC.
2. SEE 1104-00-3335 FOR SCHEMATIC.
1. MANUFACTURER'S MARKING INDICATES CORRECT ORIENTATION OF CONNECTOR.

NOTE UNLESS OTHERWISE SPECIFIED

| REV | ECO | BY | DATE | APP |
|---|---|---|---|---|
| | | | | |

SEE VIEW D FOR ASSEMBLY

SEE VIEW B FOR ASSEMBLY




INSTALL HEATSINKS ON U6 AND U7 BEFORE SOLDERING SEE VIEW A

CAD JOB #: B055F

| | | | |
|---|---|---|---|
| REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN: Amy Talmadge | DATE | WAVETEK SAN DIEGO, CALIFORNIA |
| MATERIAL | CHECKED | | TITLE: PCA, OUTPUT BOARD |
| | PROJ ENGR | | |
| FINISH: WAVETEK PROCESS | RELEASE APPROV | | |
| DO NOT SCALE DRAWING | UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ± .XXX ± | | SIZE: D; FSCM NO: 23338; DWG NO: 1101-00-3335; REV: J; SCALE: ; MODEL: SERIES; SHEET: OF |

1101-00-3335 J

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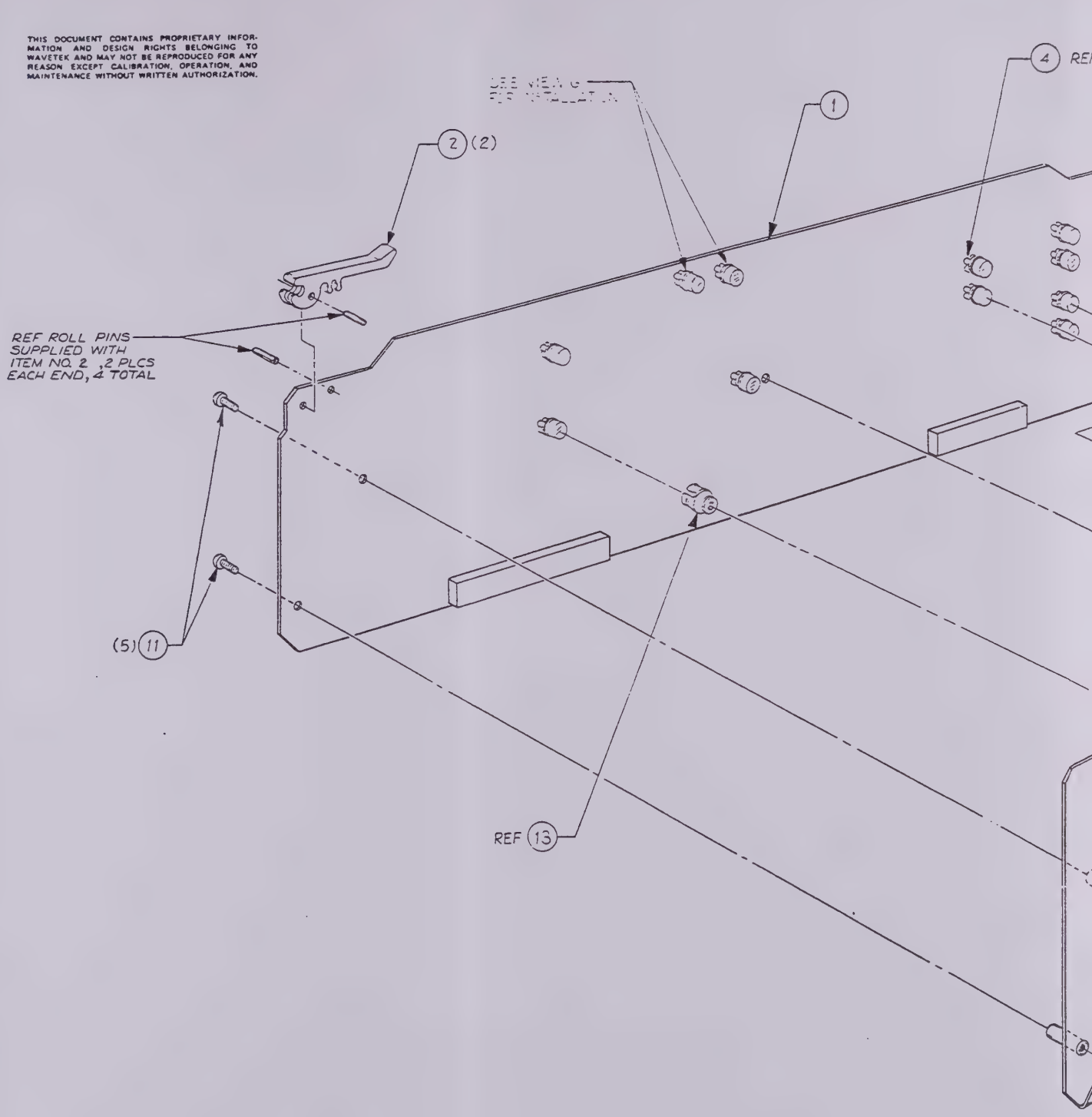
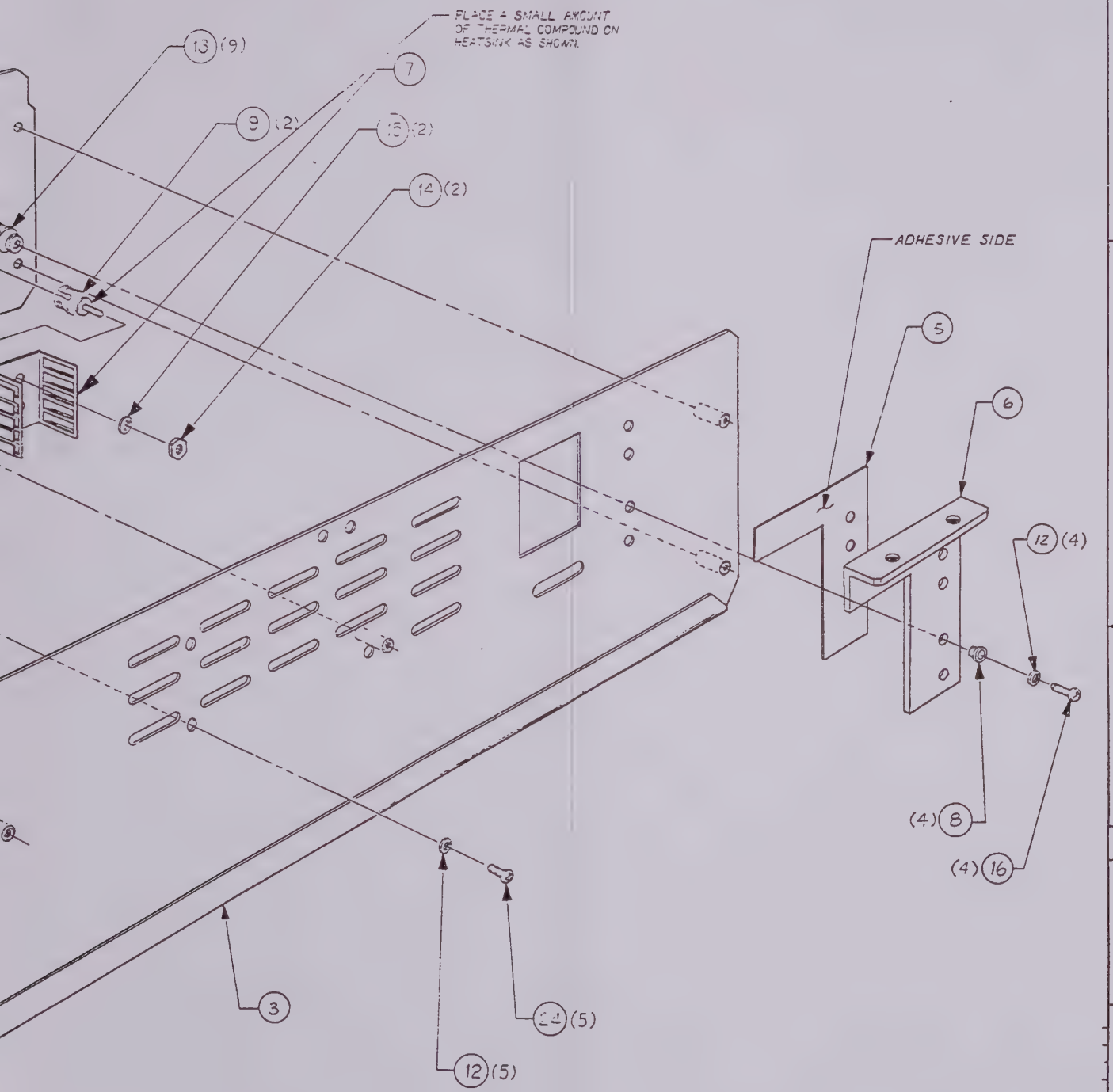



NOTE UNLESS OTHERWISE SPECIFIED

8 7 6 5

| REV | ECN | BY | DATE | APP |
|---|---|---|---|---|




| | | | |
|---|---|---|---|
| REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN S.C / A.T. | DATE 7/90 | WAVETEK SAN DIEGO, CALIFORNIA |
| MATERIAL | PROJENGR | 7/90 | TITLE PCA, OUTPUT BOARD |
| | RELEASE APPROV | 7/90 | |
| FINISH WAVETEK PROCESS | TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1° XX ±.030 | | |
| | DO NOT SCALE DWG | MODEL NO 90 SERIES | DWG NO 1101-00-3335 REV J |
| | SCALE NONE | CODE IDENT 23338 | SHEET 3 OF 3 |

1101-00-3335 J

4 3 2 1

D C B A

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| REFERENCE DESIGNATORS | PART DESCRIPTION | ORIG-MFGR-PART-NO | MFGR | WAVETEK NO. | QTY/PT |
|---|---|---|---|---|---|
| 11 | SCREWS 4-40 X 3/16 | 0202-00314 | R.G. | 0202-00314 | 10 |
| CR46 | DIODE ZENER. 1N4737 1W 7.5V 10% | 1N4737A | MOT | 0374-00082 | 1 |
| R162 R166 | RES. MF, 1/2W, 1%, 365 OHM | RN65D3650F | DALE | 0388-03650 | 2 |
| REF | MODEL 90 SUB-ASY FUNCTION TEST PROCESS | 1008-00-0396-1 | WVTK | 1008-00-0396-1 | 1 |
| NONE | A/D. OUTPUT BOARD | 1101-00-3335 | WVTK | 1101-00-3335 | 1 |
| NONE | SCHEMATIC. OUTPUT BD | 1104-00-3335 | WVTK | 1104-00-3335 | 1 |
| U12 | U: CURRENT AMP, 100MA | LH0002CN | NSC | 120 1022 | 1 |
| CR14 | SL ZR 6.2V 5% 400MW (1N753A) | 1N753A | ROHM | 131.9620 | 1 |
| 3 | SHIELD. OUT PUT BOARD | 1400-02-3066 | WVTK | 1400-02-3066 | 1 |
| 6 | HEAT SINK. OUT PUT BOARD | 1400-02-3067 | WVTK | 1400-02-3067 | 1 |
| 5 | THERMAL GASKET. OUT PUT BOARD | 1400-02-3068 | WVTK | 1400-02-3068 | 1 |
| 7 | HEAT SINK. MODIFICATION | 1400-02-3085 | WVTK | 1400-02-3085 | 1 |
| C33 C35 | CAP, CER, 100PF, 100V, AXIAL | CAC02C0G101J100A(OBS) | CORNG | 1500-01-0106 | 2 |

| WAVETEK PARTS LIST | TITLE | ASSEMBLY NO. | REV |
|---|---|---|---|
| | PCA. OUTPUT BOARD | 1100-00-3335 | AC |

PAGE 1

| REFERENCE DESIGNATORS | PART DESCRIPTION |
|---|---|
| C103T C6 | CAP CER 47PF 200V 5% AXIAL |
| C19 | CAP, CER, 56PF, 100V, 5%, AXIAL |
| C31 | CAP, CER, 82PF, 100V, 5%, COG, AXIAL |
| C71 C72 C73 C74 | CAP, MICA, 910PF, 100V, 1%, RADIAL |
| C29 C30 C46 C47 C38 C60 | CAP, ELECT, 10MF/25V RADIAL LEAD, SP .10 |
| C4 C5 | CAP, ELECT, 100MF, 35V RADIAL LEAD, SP .20 |
| C1 C2 C3 | CAP, ELEC, 100 MF, 16V, RAD, .1 LS |
| C15 C18 | CAP, ELECT, 220MF/10V |
| C11 C9 | CAP, ELECT, 22MF, 25V, RADIAL |
| C69 C70 | CO5 CAP, MET POLY, .1MF, 100V/160V DC, .4 LS |
| C28 | CAP, TANT, 100MF, 10V |
| C24 C25 | CAP, TANT, 2.2MF, 25V |

| WAVETEK PARTS LIST | TITLE |
|---|---|
| | PCA. OUTPUT BOARD |

| REFERENCE DESIGNATORS | PART DESCRIPTION | ORIG-MFGR-PART-NO | MFGR | WAVETEK NO. | QTY/PT |
|---|---|---|---|---|---|
| C104 C20 C21 C34 C35 C36 C38 C39 C43 C49 C50 C51 C54 C55 C10 C103 C106 C107 C13 C14 C16 C17 C22 C23 C32 C33 C37 C43 C44 C48 C34 C36 C37 C65 C66 C67 C68 C7 C76 C77 C79 C8 C80 C81 C82 C83 C84 C85 C86 C87 C88 C89 C90 C91 C95 C96 C97 C98 | CAP CER MON .01MF 50V, AXIAL | CAC02Z5U103Z100A | CORNG | 1500-01-0310 | 13 |
| | CAP, CER, MON, .1MF, 50V, AXIAL | CAC03Z5U104Z050A | CORNG | 1500-01-0405 | 44 |
| E26 | CAP, CER, 120PF 200V 5% AXIAL | SA102A121JAA | AVX | 1500-01-2106 | 1 |
| C62T | CAP, CER, 15PF, 100V, AXIAL | CAC02C0G150J100A | CORNG | 1500-01-5006 | 1 |
| C75 | CAP, CER, 1.5PF, 200V, AXIAL | SA102A1R5DAA | AVX | 1500-01-5906 | 1 |
| C41 C42 | CAP, CER, 220PF, 100V, AXIAL | CAC02C0G221J100A | CORNG | 1500-02-2106 | 2 |
| C61T | CAP, CER, 27PF, 5%, COG, 100V, AXIAL | CAC02C0G270J100A | CORNG | 1500-02-7006 | 1 |
| C63T | CAP CER 33PF 200V 5% AXIAL | CAC02C0G330J100A(OBS) | CORNG | 1500-03-3006 | 1 |
| C100T C12T C92T | CAP, CERAMIC, 3.9PF +.5PF, 200V AXIAL. | C114C399D2G5CA | KEMET | 1500-03-9906 | 3 |

| WAVETEK PARTS LIST | TITLE | ASSEMBLY NO. | REV |
|---|---|---|---|
| | PCA. OUTPUT BOARD | 1100-00-3335 | AC |

PAGE 2

| REFERENCE DESIGNATORS | PART DESCRIPTION |
|---|---|
| C40 C52 | CAP, TANT 27UF, 35V+/-10%, 0.25LS |
| C101 C102 C27 | CAP, TANT, 47MF, 20V |
| 1 | PCB. OUTPUT BOARD REF: SPEC 0008-00-0435 REV E |
| L1 L2 | INDUCTOR, 2.2 MHY, 40MA, RADIAL |
| J11 | CONN, HEADER, 24 PIN, RECPT, 2X12, .1 CTR, PCMT |
| J10 | CONN, HEADER, 40 PIN, RECPT, 2X20, .1 CTR PCMT |
| TP3 TP5 | TEST POINT, BLK, PC |
| TP1 TP10 TP11 TP12 TP2 TP4 TP6 TP7 TP8 TP9 | TEST POINT, RED, PC |
| P35 | CONN, SUB MIN |
| 20 | SPACER, COMP, MUNTING, .085OD, .032ID, .300LG |
| 2 | PC BD EJECTOR |

| WAVETEK PARTS LIST | TITLE |
|---|---|
| | PCA. OUTPUT BOARD |

NOTE UNLESS OTHERWISE SPECIFIED

8 7 6 5

| REV | ECO | BY | DATE | APP |
|---|---|---|---|---|

| RIG-MFGR-PART-NO | MFGR | WAVETEK NO. | QTY/PT |
|---|---|---|---|
| AC02C0G470J100A(OBS) | CORNG | 1300-04-7006 | 2 |
| AC02C0G560J100A | CORNG | 1300-05-6000 | 1 |
| A101A820JAA | AVX | 1300-08-2006 | 1 |
| M15-911F | ARCO | 1300-19-1101 | 4 |
| RE 10/63 | NIC | 1300-31-0002 | 6 |
| RE101M35V10X12.5(OBS) | NIC | 1300-31-0102 | 2 |
| RE101M16V6.3X11 | NIC | 1300-31-0111 | 3 |
| CEA1AU221 | PANAS | 1300-32-2001 | 2 |
| RA25VB22RM6X7LL | UNCON | 1300-32-2002 | 2 |
| 300-41-0445 | WVTK | 1300-41-0434 | 2 |
| 299D107X9010EE4 | SPRAG | 1300-71-0711 | 1 |
| 299D225X9025AA2 | SPRAG | 1300-72-2302 | 2 |

| REFERENCE DESIGNATORS | PART DESCRIPTION | ORIG-MFGR-PART-NO | MFGR | WAVETEK NO. | QTY/PT |
|---|---|---|---|---|---|
| 4 | TRANSIPAD | 531-218 | BIVAR | 2800-11-0004 | 11 |
| 9 | HEATSINK | 2606SH5E | WAKE | 2800-11-0012 | 2 |
| 8 | WASHER | 5607-150 | SESTH | 2800-11-0015 | 4 |
| 13 | HEATSINK, TO5, EPOXY INS | 260-4T5E | WAKE | 2800-11-0031 | 9 |
| 10 | HEATSINK, 14-16 PIN DIP, ALUM, BLK AN, CLIPON | 58028 | AAVID | 2800-11-0034 | 2 |
| 14 | NUT, HEX, 6-32, Z | MS35649-264 | COML | 2800-14-6100 | 2 |
| 24 | SCREW, 4-40X3/16 PHP, Z 4-40 X 3/16 | 4-40X3/16 PLPS PAN | CMRCL | 2800-38-4103 | 5 |
| 12 | WASHER, LOCK REG, S/S #4 | MS 35338-135 | CMRCL | 2800-45-4000 | 9 |
| 15 | WASHER, LOCK, REG S/S #6 | MS 35338-136 | CMRCL | 2800-45-6000 | 2 |
| 16 | SCREW PLPS PAN M/S 18-8 S/S 4-40X3/8 | MS 51957-15 | CMRCL | 2800-48-4106 | 4 |
| FB6 | FERRITE BEAD | 56-590-65/3B | FERRX | 3100-00-0001 | 1 |
| FB1 FB2 FB3 | BALUN CORE, FERRITE, 680 OHMS | 2943666671 | FARIT | 3100-00-0017 | 3 |
| FB10 FB9 | FERRITE BEAD | 2673004701 | FRITE | 3100-00-0020 | 2 |

| | | | |
|---|---|---|---|
| | ASSEMBLY NO. 1100-00-3335 | | REV AC |
| | PAGE 3 | | |
| WAVETEK PARTS LIST | TITLE PCA, OUTPUT BOARD | ASSEMBLY NO. 1100-00-3335 | REV AC |
| | | PAGE 5 | |

| RIG-MFGR-PART-NO | MFGR | WAVETEK NO. | QTY/PT |
|---|---|---|---|
| 299D276X9035FE4 | SPRAG | 1300-72-7602 | 2 |
| 296D476X9020PE4(OBS) | SPRAG | 1300-74-7601 | 3 |
| 1700-00-3335 | WVTK | 1700-00-3335 | 1 |
| 331LY-222J | TOKO | 1800-00-0046 | 2 |
| 1-0102384-7(REF ONLY) | AMP | 2100-02-0235 | 1 |
| 1-0102385-2(REF ONLY) | AMP | 2100-02-0256 | 1 |
| P-104-01-00 | COMPO | 2100-04-0054 | 2 |
| P-104-01-02 | COMPO | 2100-04-0055 | 10 |
| 7-848 | AMPH | 2100-07-0011 | 1 |
| 38.300" | BIVAR | 2800-04-0024 | 4 |
| 7-2-C | BRIT | 2800-07-0032 | 2 |

| REFERENCE DESIGNATORS | PART DESCRIPTION | ORIG-MFGR-PART-NO | MFGR | WAVETEK NO. | QTY/PT |
|---|---|---|---|---|---|
| 23 | INSULATOR, THERMAL, SELF ADHESIVE .510 OD x .140 ID. .009 THK | 7403-09AC-19 | BERGQ | 3100-00-0022 | 2 |
| K5 | RELAY, 2 FORMC, 5V, DIP 14 | DF2E-DC5V | AROMT | 4300-00-0033 | 1 |
| K1 K2 K3 K4 K6 K7 | RELAY, 1 FORMC, 5V, .312H, .296W | HD1E-M-DC5V | AROMT | 4300-00-0034 | 6 |
| R84 R86 R87 | POT, TRIM, 100 | 3329H-1-101 | BOURN | 4600-01-0100 | 3 |
| R67 R70 | POT, 1 TURN, SIDE TRIM, 1/4" DIA, 100ohm | 3329W-1-101 | BOURN | 4601-01-0101 | 2 |
| R69 | POT, 1 TURN, SIDE TRIM, 1/4" DIA, 500 OHM | 3329W-1-501 | BOURN | 4601-01-0500 | 1 |
| R25 | POT, SIDE TRIM, 20T, 2K | 68WR2K | BECK | 4609-90-0010 | 1 |
| R146 | POT, SIDE TRIM, 20T, 20K | 68WR20K | BECK | 4609-90-0011 | 1 |
| R138 | POT, SIDE TRIM, 20T, 500 | 68WR500 | BECK | 4609-90-0014 | 1 |
| R9 | POT, SIDE TRIM, 20T, 100 | 68WR100 | BECK | 4609-90-0017 | 1 |
| R73 R74 R75 R76 R91 R92 R93 R94 | RES, C, 1/2W, 5%, 10 | RC-1/2-10J | STKPL | 4700-25-0100 | 8 |
| R62 R78 | RES, C, 1/2W, 5%, 1K | RC-1/2-102J | STKPL | 4700-25-1001 | 2 |
| R11 R13 | RES, C, 1/2W, 5%, 220 | RC-1/2-221J | STKPL | 4700-25-2200 | 2 |

| | | | |
|---|---|---|---|
| | ASSEMBLY NO. 1100-00-3335 | | REV AC |
| | PAGE 4 | | |
| WAVETEK PARTS LIST | TITLE PCA, OUTPUT BOARD | ASSEMBLY NO 1100-00-3335 | REV AC |
| | | PAGE 6 | |

| | | | |
|---|---|---|---|
| REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN | DATE | WAVETEK San Diego, California |
| MATERIAL | CHECKED | | TITLE PARTS LIST OUTPUT BOARD |
| | PROJ ENGR | | |
| | RELEASE APPROV | | |
| FINISH WAVETEK PROCESS | UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES .XX ± .XXX ± | | SIZE D FSCM NO 23338 DWG NO 1100-00-3335 REV AC |
| DO NOT SCALE DRAWING | | | SCALE MODEL 90 SHEET 1 OF 2 |

4 3 2 1

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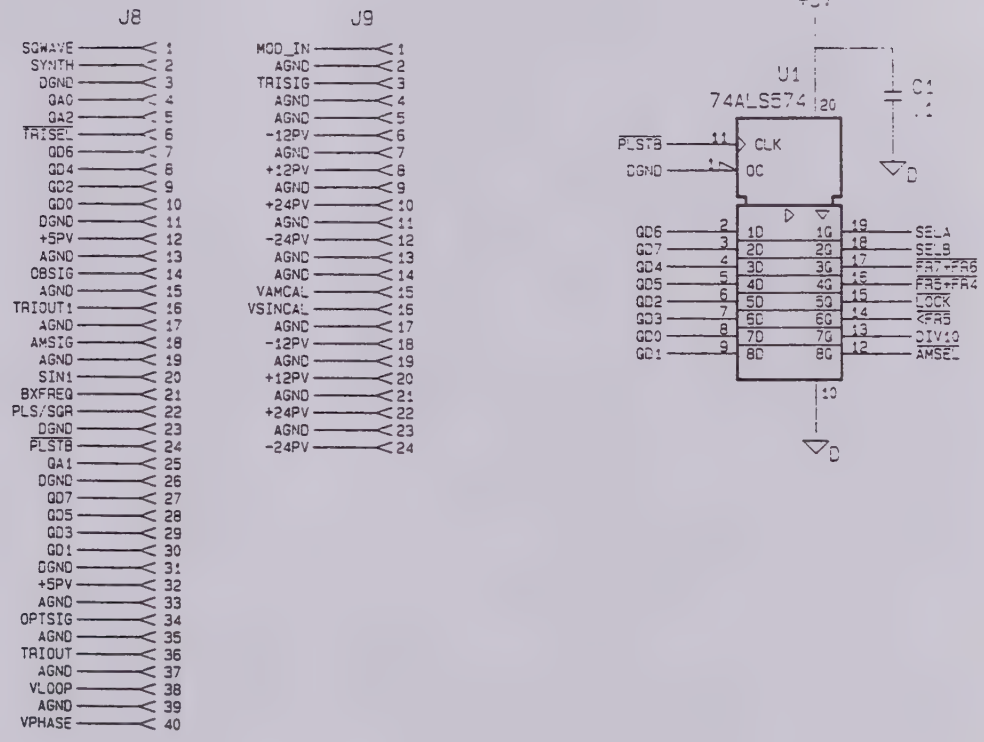
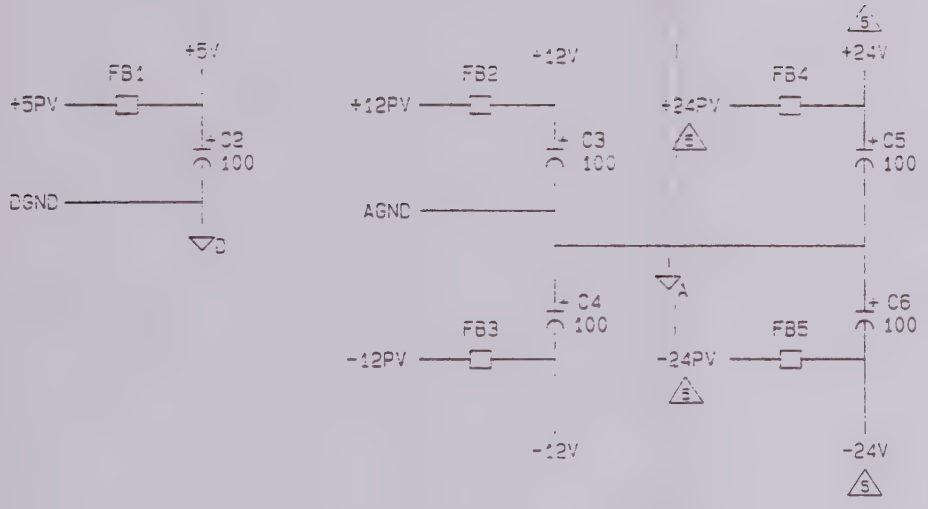



6. * = MATCHED DIODE SET 4898-00-0015.
5. $\perp_A$ = ANALOG GROUND SYMBOL.
4. $\perp_D$ = DIGITAL GROUND SYMBOL.
3. ALL CAPACITORS ARE IN MICROFARADS (uF).
2. ALL RESISTORS ARE IN OHMS, 1/8W, 1%, MF.
1. FOR ASSEMBLY INTERCONNECTION, SEE INSTRUMENT SCHEMATIC.

NOTE UNLESS OTHERWISE SPECIFIED

| REV | ECO | BY | DATE | APP |
|---|---|---|---|---|
| A | ECO [illegible] | | | |
| B | ECO 91-121 | [illegible] | [illegible] | |
| C | [illegible] | [illegible] | [illegible] | |
| D | [illegible] | [illegible] | [illegible] | |




CAD JOB #: B0630

| | | | |
|---|---|---|---|
| REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN A.C.T. | DATE 7/90 | WAVETEK SAN DIEGO, CALIFORNIA |
| MATERIAL | CHECKED | | TITLE |
| | PROJ ENGR | | SCHEMATIC, PHASE LOCK LOOP |
| FINISH WAVETEK PROCESS | RELEASE APPROV | | |
| DO NOT SCALE DRAWING | UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES .XX: .XXX: : | | SIZE D · FSCM NO 23338 · DWG. NO. 1104-00-3437 · REV C · SCALE NONE · MODEL 90 SERIES · SHEET 1 OF 6 |

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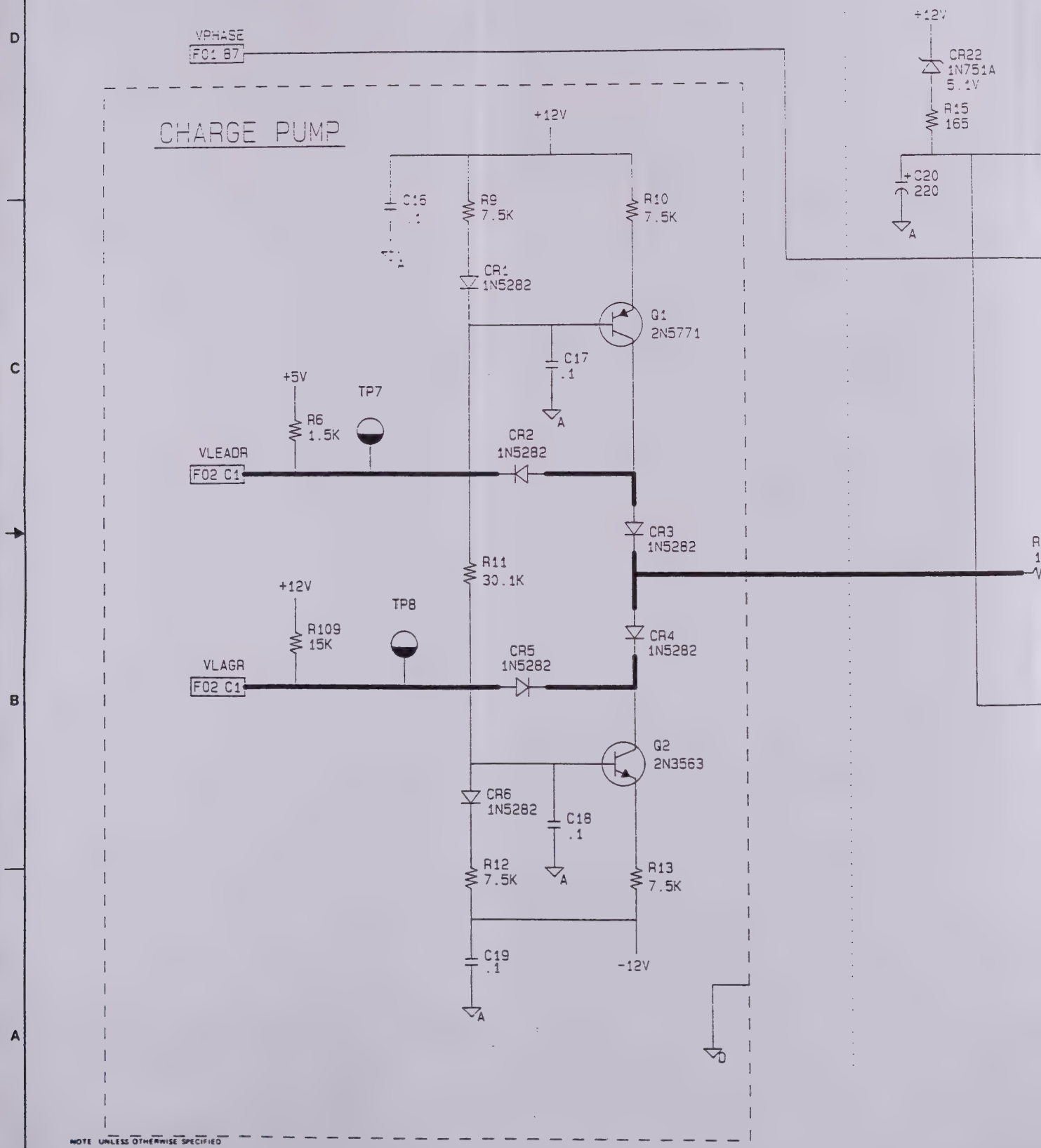

LOCK LOOP FILTER
REV
ECO
BY
DATE
APP
R16
7.5K
R17
7.5K
C24
1
C21
4.7
R23
5.49K
C25
220
C26
220
+5V
+12V
U7A
DG211
-12V
R30
2.49K
FR5+FR4
C5 F01
C34
.1
R18
7.5K
R19
7.5K
C22
1
C27
.0047
R24
5.49K
C28
2.2
C29
2.2
U7D
R28
2.49K
FR7+FR6
C5 F01
C33
.1
C73
470pF
R130
7.5K
C74
.01
R32
2.49K
LOCK
C5 F01
C36
.1
C30
.1
+12V
TP9
PLLER
R20
1K
C23
.01
R27
10
R29
110K
U6
MC34081P
U7B
VLOOP
C5 F01
C31
4.7
C32
.1
-12V
R21
750
R22
750
C38
10
C37
10
R31
2.49K
<FR5
C5 F01
C39
.1
U7C
CAD JOB # 80810
REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DO NOT SCALE DRAWING
DRAWN A.C.T.
DATE 7/90
CHECKED
PROJ ENGR
RELEASE APPROV
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES
WAVETEK SAN DIEGO, CALIFORNIA
TITLE
SCHEMATIC, PHASE LOCK LOOP
SIZE D
FSCM NO 23338
DWG NO 1104-00-3437
REV C
SCALE NONE
MODEL 90 SERIES
SHEET 3 OF 6
1104-00-3437

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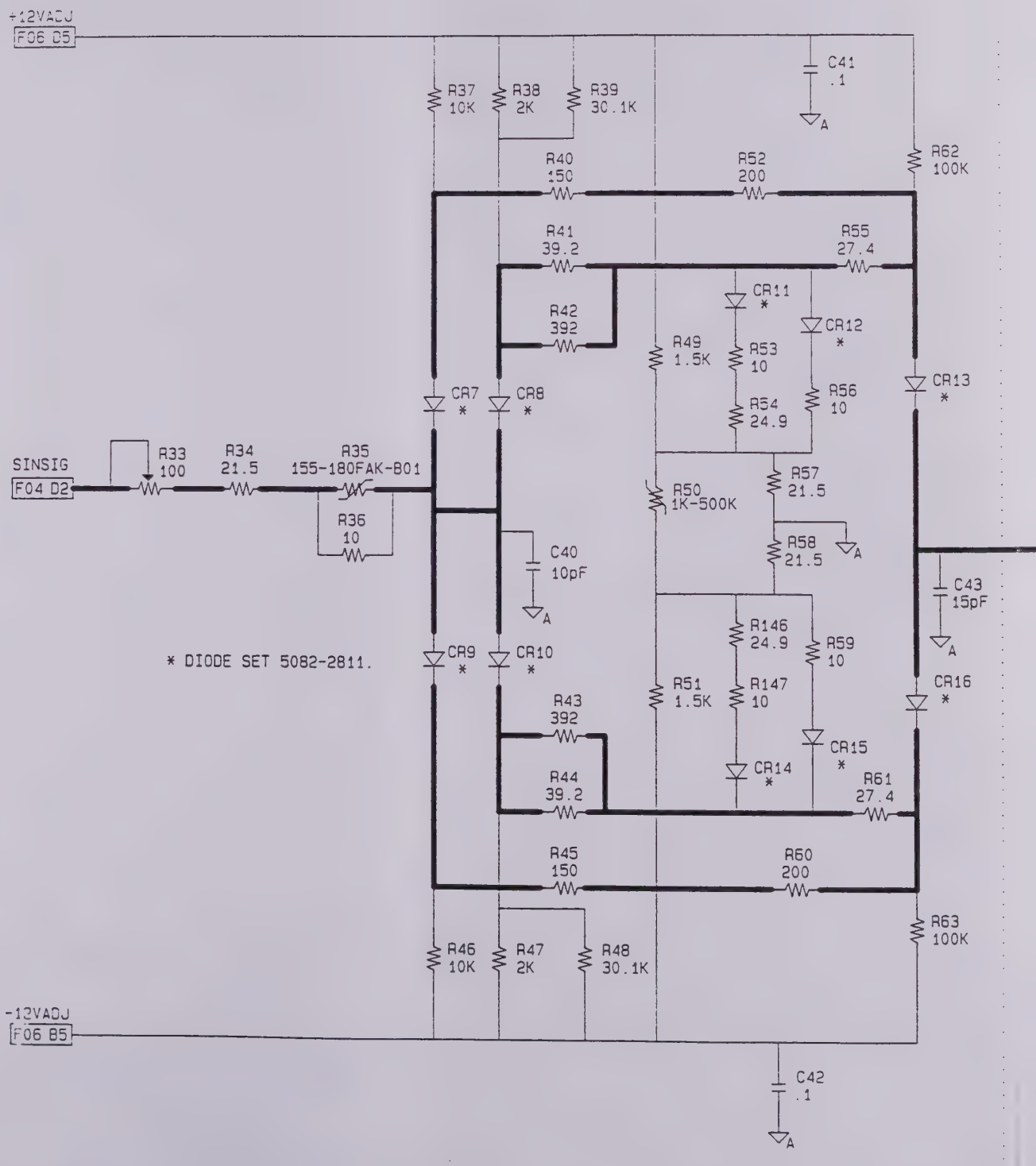
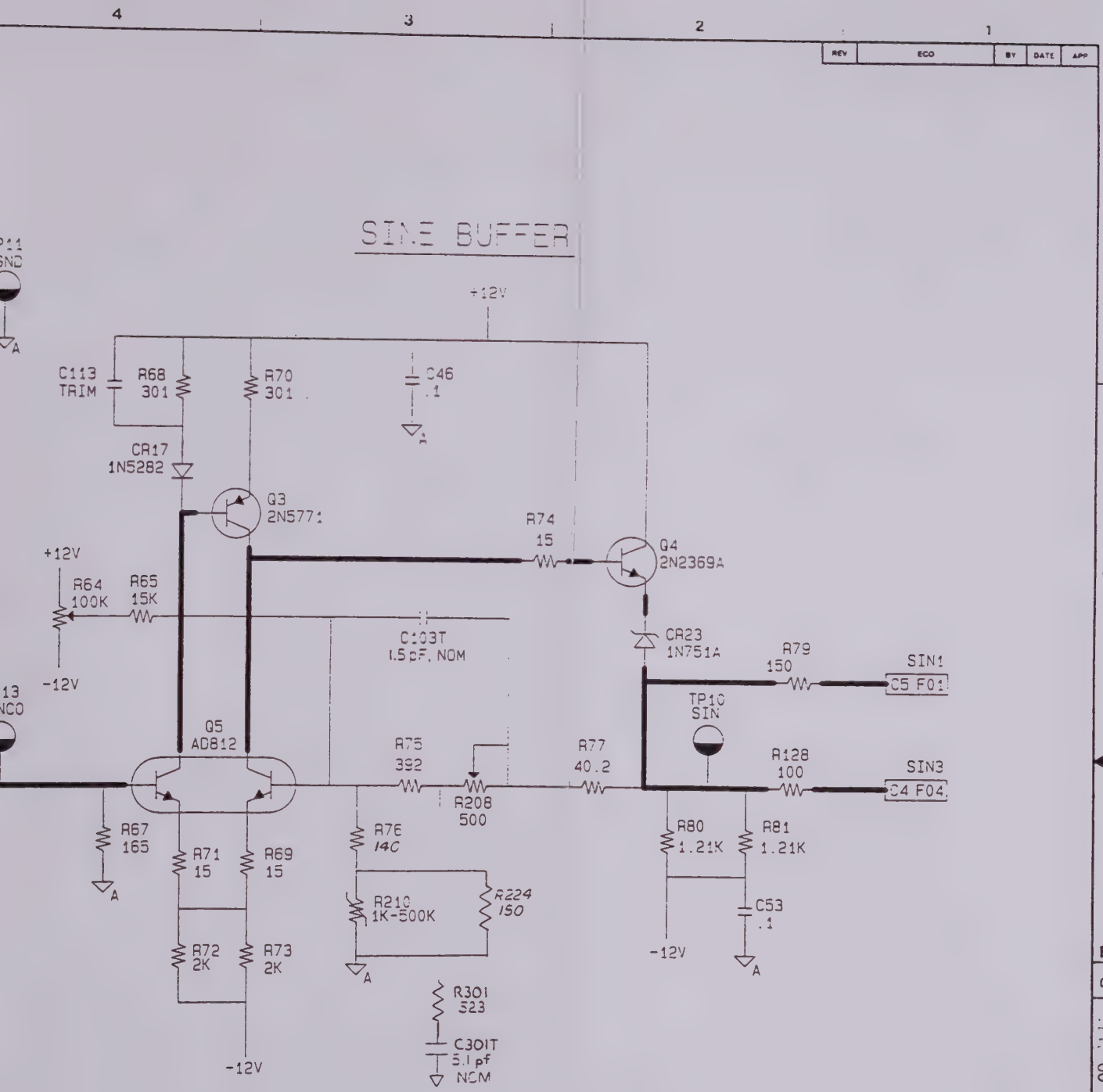
# SINE CONVERTER




NOTE UNLESS OTHERWISE SPECIFIED


SINE BUFFER
+12V
C113
TRIM
R68
301
R70
301
C46
.1
CR17
1N5282
Q3
2N5771
R74
15
Q4
2N2369A
+12V
R64
100K
R65
15K
-12V
C103T
1.5pF, NOM
CR23
1N751A
R79
150
SIN1
C5 F01
TP10
SIN
Q5
AD812
R75
392
R208
500
R77
40.2
R128
100
SIN3
C4 F04
R67
165
R71
15
R69
15
R76
140
R80
1.21K
R81
1.21K
R210
1K-500K
R224
150
C53
.1
R72
2K
R73
2K
-12V
R301
523
C301T
5.1pf
NOM
REV
ECO
BY
DATE
APP
REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH
WAVETEK PROCESS
DO NOT SCALE DRAWING
DRAWN
A. C. T.
DATE
7/90
CHECKED
E.M.
PROJ. ENGR.
RELEASE APPROV
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE
FRACTIONS DECIMALS ANGLES
WAVETEK
TITLE
SCHEMATIC,
PHASE LOCK LOOP
SIZE
D
FSCM NO
23338
DWG NO
1104-00-3437
REV
D
SCALE
NONE
MODEL 75 SERIES
SHEET 5 OF 6
1104-00-3437

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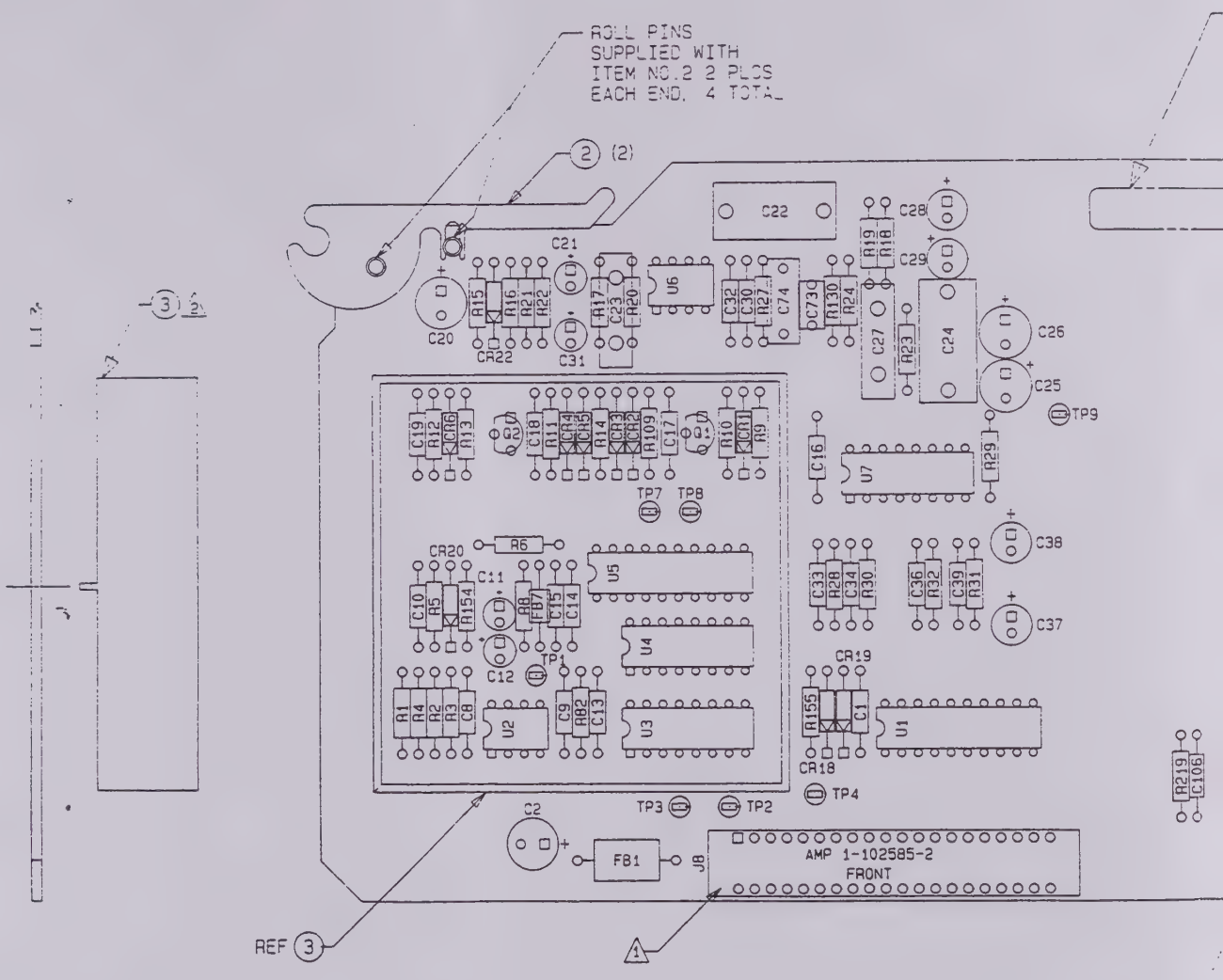
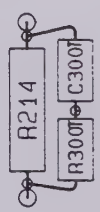


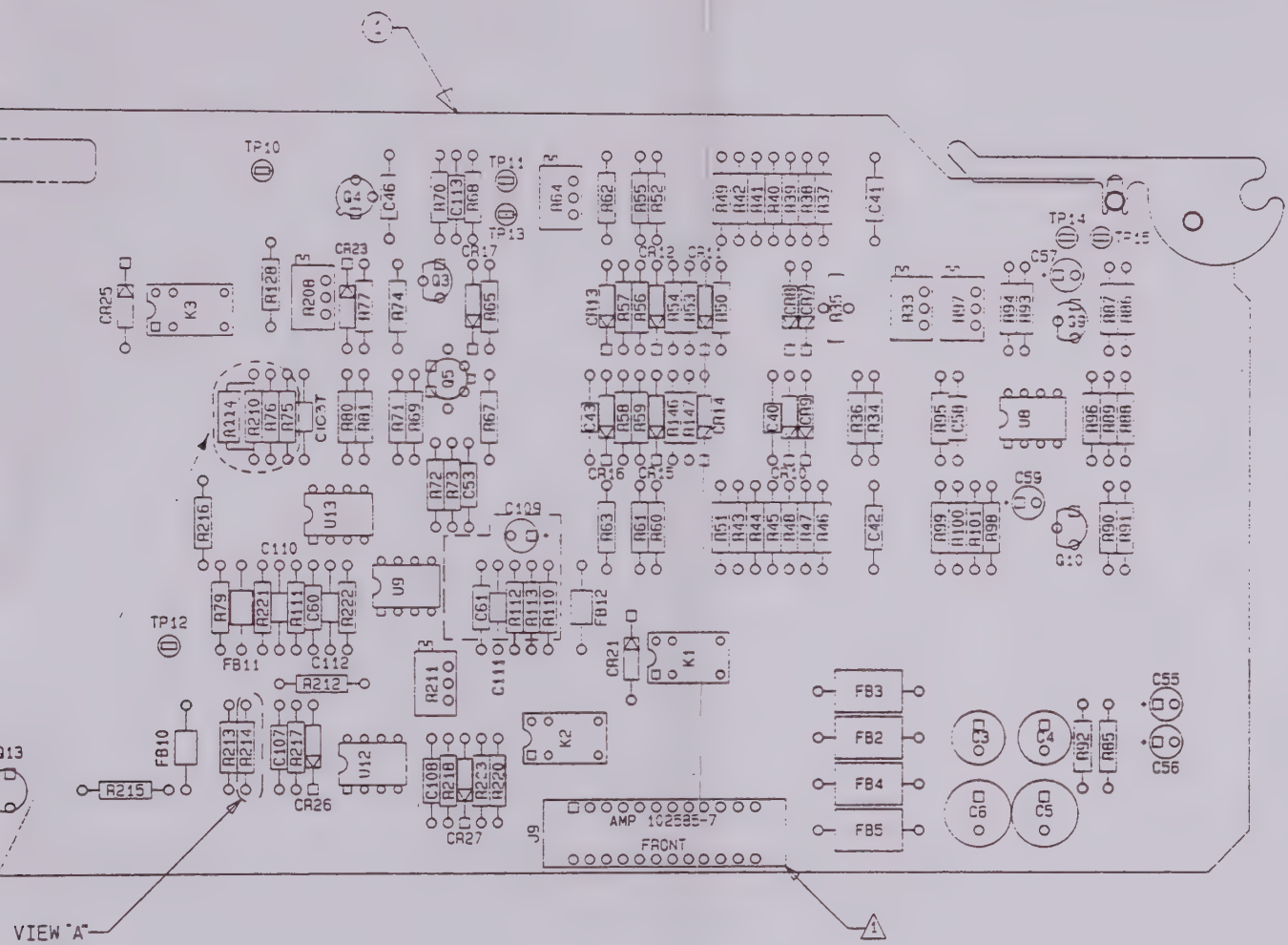

VIEW "A"
SCALE: NONE

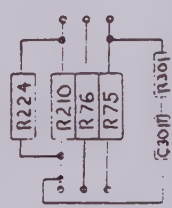
6. ASSEMBLE PER WAVETEK WORKMANSHIP STANDARDS.
5. REFERENCE DESIGNATIONS DO NOT APPEAR ON PARTS.
4. FOR ASSEMBLY INTERCONNECTION, SEE INSTRUMENT SCHEMATIC.
3. SEE 1104-00-3341 FOR SCHEMATIC.
2. INSTALL CAN FLUSH TO COMPONENT SIDE OF P.C. BOARD. SOLDER TABS ON CIRCUIT SIDE.
1. MANUFACTURER'S MARKING INDICATES CORRECT ORIENTATION OF CONNECTOR.

NOTE UNLESS OTHERWISE SPECIFIED

| REV | ECO | BY | DATE | APP |
|---|---|---|---|---|
| A | ECO 91-[illegible] FROM: 1101-00-3341 | | | |
| B | ECO-91-121 | MA | | |
| C | ECO 91-[illegible] | SC | | |
| D | ECO 91-390 | SC | | |

PLACE ASSEMBLY I.D.
LABEL IN THIS AREA




CAD JOB #: B063D

| | | | |
|---|---|---|---|
| REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN: Amy Talmadge | DATE: [illegible] | WAVETEK San Diego, California |
| MATERIAL | CHECKED: D. FISH | 6/29/90 | TITLE: PCA, PHASE LOCK LOOP BOARD |
| | PROJ ENGR: D. E. FISH | 6/29/90 | |
| FINISH: WAVETEK PROCESS | RELEASE APPROV: JM | 10/1/90 | |
| DO NOT SCALE DRAWING | UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES .XX ± .01 .XXX ± .005 | | SIZE: D; FSCM NO: 23338; DWG NO: 1101-00-3437; REV: D; SCALE: 2/1; MODEL: 90 SERIES; SHEET 1 OF 1 |

1101-00-3437 D

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| REFERENCE DESIGNATORS | PART DESCRIPTION | ORIG-MFGR-PART-NO | MFGR | WAVETEK NO. | QTY/PT |
|---|---|---|---|---|---|
| REF | MODEL 90 SUB-ASY FUNCTION TEST PROCESS | 1008-00-0396-1 | WVTK | 1008-00-0396-1 | 1 |
| NONE | A/D PHASE LOCK LOOP | 1101-00-3437 | WVTK | 1101-00-3437 | 1 |
| NONE | SCHEMATIC, PHASE LOCK LOOP | 1104-00-3437 | WVTK | 1104-00-3437 | 1 |
| R8 | RES.CFLM 4 7 OHM 5% 1/4W | 5043CX4R700J | MEPCO | 116.9471 | 1 |
| CR26 CR27 | SL ZR 6.2V 5% 400MW (1N753A) | 1N753A | ROHM | 131.9620 | 2 |
| 3 | CAN, SYNTHESIZER | 1400-02-3443 | WVTK | 1400-02-3443 | 1 |
| C112 C300T C40 | CAP CER 10PF 200V 5% AXIAL | CAC02CDG100J100A(OBS) | CORNG | 1500-01-0006 | 3 |
| C111 | CAP, CER, 100PF, 100V, AXIAL | CAC02CDG101J100A(OBS) | CORNG | 1500-01-0106 | 1 |
| C1 C10 C106 C107 C108 C13 C14 C15 C16 C17 C18 C19 C30 C32 C33 C34 C36 C39 C41 C42 C46 C53 C58 C60 C61 C8 C9 | CAP, CER, MON, .1MF, 50V, AXIAL | CAC03Z5U104Z050A | CORNG | 1500-01-0403 | 27 |
| C43 | CAP, CER, 15PF, 100V, AXIAL | CAC02CDG150J100A | CORNG | 1500-01-3006 | 1 |
| C110 | CAP, CER, 150PF, 100V, 5%, AXIAL | CAC02CDG151J100A | CORNG | 1500-01-3100 | 1 |

| WAVETEK PARTS LIST | TITLE PCA, PHASE LOCK LOOP | ASSEMBLY NO. 1100-00-3437. | REV D |
|---|---|---|---|

PAGE 1

| REFERENCE DESIGNATORS | PART DESCRIPTION | O |
|---|---|---|
| NONE | PCB, PHASE LOCK LOOP BD REF. SPEC 0008-00-0435 REV E | 1 |
| J9 | CONN, HEADER, 24 PIN, RECPT, 2X12, .1 CTR, PCMT | 0 |
| J8 | CONN, HEADER, 40 PIN, RECPT, 2X20, .1 CTR PCMT | 1 |
| TP11 TP4 | TEST POINT, BLK, PC | T |
| TP1 TP10 TP12 TP13 TP14 TP15 TP2 TP3 TP7 TP8 TP9 | TEST POINT, RED, PC | T |
| 2 | PC BD EJECTOR | 8 |
| FB1 FB2 FB3 FB4 FB5 | BALUN CORE, FERRITE, 680 OHMS | 2 |
| FB10 FB11 FB12 FB7 | BALUN CORE, FERRITE, 82 OHMS | 2 |
| K1 K2 K3 | RELAY, 1 FORMC, 5V, .312H, .296W | K |
| R64 | POT, SIDE TRIM, 20T, 100K | 4 |
| R208 | POT, SIDE TRIM, 20T, 300 | 4 |

| WAVETEK PARTS LIST | TITLE PCA, PHASE LOCK LOOP |
|---|---|

| REFERENCE DESIGNATORS | PART DESCRIPTION | ORIG-MFGR-PART-NO | MFGR | WAVETEK NO. | QTY/PT |
|---|---|---|---|---|---|
| C103T | CAP, CER, 1.5PF, 200V, AXIAL | SA102A1R5DAA | AVX | 1500-01-3906 | 1 |
| C73 | CAP, CER, 470PF, 1KV | DD-471 | CRL | 1500-04-7111 | 1 |
| C301T | CAP, CER, 5.1PF, 200V, AXIAL | SA102A5R1DAA | AVX | 1500-05-1906 | 1 |
| C37 C38 | CAP, ELECT, 10MF, 20%, 16V, END MOUNT | 3477CB100M016JMBS | MEPCO | 1500-31-0001 | 2 |
| C5 C6 | CAP, ELECT, 100MF, 35V RADIAL LEAD, SP .20 | NRE101M35V10X12.5(OBS) | NIC | 1500-31-0102 | 2 |
| C2 C3 C4 | CAP, ELECT, 100MF, 25V, RADIAL LEAD-SP SIZE | NRE101M25V6.3X11 | NIC | 1500-31-0122 | 3 |
| C20 C25 C26 | CAP, ELECT, 220MF, 20%, 16V, RADIAL END MOUNT, 0.14 LEAD SPACE | 16TWSS220M | RUBY | 1500-32-2104 | 3 |
| C11 C12 C21 C31 C35 C36 C37 C39 | CAP, ELECT, 4.7MF/50V RADIAL LEAD, SP .10 | ECEA1HV4R7SC | PANAS | 1500-34-7903 | 8 |
| C23 C74 | CAP, MYLAR, .01MF, 100V | 225P10391WD3 | SPRAG | 1500-41-0314 | 2 |
| C22 C24 | CAP, MYLAR, 1MF, 100V, RADIAL | PMT2R1.0K100 | ITT | 1500-41-0524 | 2 |
| C27 | CAP, MYLAR, .0047MF, 100V, RADIAL | 225P47291WD3 | SPRAG | 1500-44-7204 | 1 |
| C109 C28 C29 | CAP, TANT, 2.2MF, 25V | 199D225X9025AA2 | SPRAG | 1500-72-2302 | 3 |

| WAVETEK PARTS LIST | TITLE PCA, PHASE LOCK LOOP | ASSEMBLY NO. 1100-00-3437 | REV D |
|---|---|---|---|

PAGE 2

| REFERENCE DESIGNATORS | PART DESCRIPTION | C |
|---|---|---|
| R97 | POT, SIDE TRIM, 20T, 1K | 4 |
| R211 R33 | POT, SIDE TRIM, 20T, 100 | 4 |
| R128 R213 R216 R221 R85 R92 | RES, MF, 1/8W, 1%, 100 | 1 |
| R14 R20 | RES, MF, 1/8W, 1%, 1K | 1 |
| R217 R218 R219 R37 R46 | RES, MF, 1/8W, 1%, 10K | 1 |
| R62 R63 | RES, MF, 1/8W, 1%, 100K | 1 |
| R147 R212 R222 R27 R36 R53 R56 R59 | RES, MF, 1/8W, 1%, 10 | 1 |
| R29 | RES, MF, 1/8W, 1%, 110K | 1 |
| R220 | RES, MF, 1/8W, 1%, 121 | 1 |
| R80 R81 | RES, MF, 1/8W, 1%, 1.21K | 1 |
| R94 R98 | RES, MF, 1/8W, 1%, 12.1K | 1 |
| R76 | RES, MF, 1/8W, 1%, 140 | 1 |
| R224 R40 R45 R79 | RES, MF, 1/8W, 1%, 150 | 1 |
| R49 R51 R6 | RES, MF, 1/8W, 1%, 1.5K | 1 |
| R109 R63 | RES, MF, 1/8W, 1%, 15K | 1 |
| R134 R69 R71 R74 | RES, MF, 1/8W, 1%, 15 | 1 |

| WAVETEK PARTS LIST | TITLE PCA, PHASE LOCK LOOP |
|---|---|

NOTE UNLESS OTHERWISE SPECIFIED

8 7 6 5

| REV | ECO | BY | DATE | APP |
|---|---|---|---|---|

| C-MFGR-PART-NO | MFGR | WAVETEK NO. | QTY/PT |
|---|---|---|---|
| )0-00-3341 | WVTK | 1700-00-3341 | 1 |
| )102584-7(REF ONLY) | AMP | 2100-02-0255 | 1 |
| )102585-2(REF ONLY) | AMP | 2100-02-0256 | 1 |
| -104-01-00 | COMPO | 2100-04-0034 | 2 |
| -104-01-02 | COMPO | 2100-04-0035 | 11 |
| -2-C | BRIT | 2800-07-0032 | 2 |
| 43666671 | FARIT | 3100-00-0017 | 5 |
| 43015111 | FRITE | 3100-00-0018 | 4 |
| 1E-M-DC3V | AROMT | 4300-00-0034 | 3 |
| XR100K | BECK | 4609-90-0012 | 1 |
| XR500 | BECK | 4609-90-0014 | 1 |

| ASSEMBLY NO. 1100-00-3437 | REV D |
|---|---|
| PAGE 3 | |

| REFERENCE DESIGNATORS | PART DESCRIPTION | ORIG-MFGR-PART-NO | MFGR | WAVETEK NO | QTY/PT |
|---|---|---|---|---|---|
| R13 R67 | RES. MF. 1/8W. 1%. 165 | RN55D-1650F | TRW | 4701-03-1650 | 2 |
| R2 R52 R60 | RES. MF. 1/8W. 1%. 200 | RN55D-2000F | TRW | 4701-03-2000 | 3 |
| R101 R38 R47 R72 R73 R96 | RES. MF. 1/8W. 1%. 2K | RN55D-2001F | TRW | 4701-03-2001 | 6 |
| R34 R57 R58 | RES. MF. 1/8W. 1%. 21.5 | RN55D-21R5F | TRW | 4701-03-2159 | 3 |
| R300T | RES. MF. 1/8W. 1%. 249 | RN55D-2490F | TRW | 4701-03-2490 | 1 |
| R28 R3 R30 R31 R32 R95 | RES. MF. 1/8W. 1%. 2.49K | RN55D-2491F | TRW | 4701-03-2491 | 6 |
| R146 R34 | RES. MF. 1/8W. 1%. 24.9 | RN55D-24R9F | TRW | 4701-03-2499 | 2 |
| R55 R61 | RES. MF. 1/8W. 1%. 27.4 | RN55D-27R4F | TRW | 4701-03-2749 | 2 |
| R113 | RES. MF. 1/8W. 1%. 2.94K | 5033RD2K490F | MEPCO | 4701-03-2941 | 1 |
| R1 R68 R70 | RES. MF. 1/8W. 1%. 301 | RN55D-3010F | TRW | 4701-03-3010 | 3 |
| R11 R39 R48 | RES. MF. 1/8W. 1%. 30.1K | RN55D-3012F | TRW | 4701-03-3012 | 3 |
| R223 | RES. MF. 1/8W. 1%. 30.1 | RN55D-30R1F | TRW | 4701-03-3019 | 1 |
| R110 | RES. MF. 1/8W. 1%. 3.32K | RN55D-3321F | TRW | 4701-03-3321 | 1 |
| R155 R4 R42 R43 R75 | RES. MF. 1/8W. 1%. 392 | RN55D-3920F | TRW | 4701-03-3920 | 5 |
| R41 R44 | RES. MF. 1/8W. 1%. 39.2 | RN55D-39R2F | TRW | 4701-03-3929 | 2 |
| R77 | RES. MF. 1/8W. 1%. 40.2 | RN55D-40R2F | TRW | 4701-03-4029 | 1 |

| WAVETEK PARTS LIST | TITLE PCA. PHASE LOCK LOOP | ASSEMBLY NO. 1100-00-3437 | REV D |
|---|---|---|---|
| | | PAGE 5 | |

| IG-MFGR-PART-NO | MFGR | WAVETEK NO. | QTY/PT |
|---|---|---|---|
| XR1K | BECK | 4609-90-0015 | 1 |
| XR100 | BECK | 4609-90-0017 | 2 |
| 55D-1000F | TRW | 4701-03-1000 | 6 |
| 55D-1001F | TRW | 4701-03-1001 | 2 |
| 55D-1002F | TRW | 4701-03-1002 | 5 |
| 55D-1003F | TRW | 4701-03-1003 | 2 |
| 43ED10R100F | MEPCO | 4701-03-1009 | 8 |
| 55D-1103F | TRW | 4701-03-1103 | 1 |
| 55D-1210F | TRW | 4701-03-1210 | 1 |
| 55D-1211F | TRW | 4701-03-1211 | 2 |
| 55D-1212F | TRW | 4701-03-1212 | 2 |
| 55D-1400F | TRW | 4701-03-1400 | 1 |
| 55D-1500F | TRW | 4701-03-1500 | 4 |
| 55D-1501F | TRW | 4701-03-1501 | 3 |
| 55D-1502F | TRW | 4701-03-1502 | 2 |
| 55D-15R0F | TRW | 4701-03-1509 | 4 |

| ASSEMBLY NO. 1100-00-3437 | REV D |
|---|---|
| PAGE 4 | |

| REFERENCE DESIGNATORS | PART DESCRIPTION | ORIG-MFGR-PART-NO | MFGR | WAVETEK NO. | QTY/PT |
|---|---|---|---|---|---|
| R213 R214 | RES. MF. 1/8. 1%. 499 | RN55D-4990F | TRW | 4701-03-4990 | 2 |
| R82 R86 R87 R88 R89 R90 R91 | RES. MF. 1/8W. 1%. 4.99K | RN55D-4991F | TRW | 4701-03-4991 | 7 |
| R301 | RES. MF. 1/8W. 1%. 523 | RN55D-5230F | TRW | 4701-03-5230 | 1 |
| R23 R24 | RES. MF. 1/8W. 1%. 5.49K | RN55D-5491F | MEPCO | 4701-03-5491 | 2 |
| R5 | RES. MF. 1/8W. 1%. 681 | RN55D-6810F | TRW | 4701-03-6810 | 1 |
| R100 R99 | RES. MF. 1/8W. 1%. 6.81K | RN55D-6811F | TRW | 4701-03-6811 | 2 |
| R111 | RES. MF. 1/8W. 1%. 7.15K | RN55D-7151F | TRW | 4701-03-7151 | 1 |
| R21 R22 | RES. MF. 1/8W. 1%. 750 | RN55D-7500F | TRW | 4701-03-7500 | 2 |
| R10 R12 R13 R130 R16 R17 R18 R19 R9 | RES. MF. 1/8W. 1%. 7.5K | RN55D-7501F | TRW | 4701-03-7501 | 9 |
| R93 | RES. MF. 1/8W. 1%. 8.87K | RN55D-8871F | TRW | 4701-03-8871 | 1 |
| R112T | RES. MF. 1/8W. 1%. 9.09K | RN55D-9091F | TRW | 4701-03-9091 | 1 |
| CR20 CR22 CR23 | DIODE. ZENOR. 5.1V. 500MW. GIB. IN751A | 1N751A | FAIR | 4801-01-0751 | 3 |
| CR1 CR17 CR18 CR19 CR2 CR21 CR25 CR3 CR4 CR5 CR6 | DIODE. HIGH CONDUCTANCE. ULTRA FAST | 1N5282 | FAIR | 4801-01-5282 | 11 |
| CR10 11 12 13 14 15 16 7 8 9 | DIODE SET, 5082-2811 QTY: 10: 4809-02-2811 | 4898-00-0015 | KLG | 4898-00-0015 | 1 |

| WAVETEK PARTS LIST | TITLE PCA. PHASE LOCK LOOP | ASSEMBLY NO. 1100-00-3437 | REV D |
|---|---|---|---|
| | | PAGE 6 | |

| REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN | DATE | WAVETEK San Diego, California |
|---|---|---|---|
| MATERIAL | CHECKED | | TITLE |
| | PROJ. ENGR | | PARTS LIST PHASE LOCK BOARD |
| FINISH WAVETEK PROCESS | RELEASE APPROV | | |
| DO NOT SCALE DRAWING | UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES .XX ±.01 .XXX ±.005 | | SIZE D \| FSCM NO 23338 \| DWG NO 1100-00-3437 \| REV D |
| | | | SCALE \| MODEL 90 \| SHEET 1 OF 2 |

4 3 2 1

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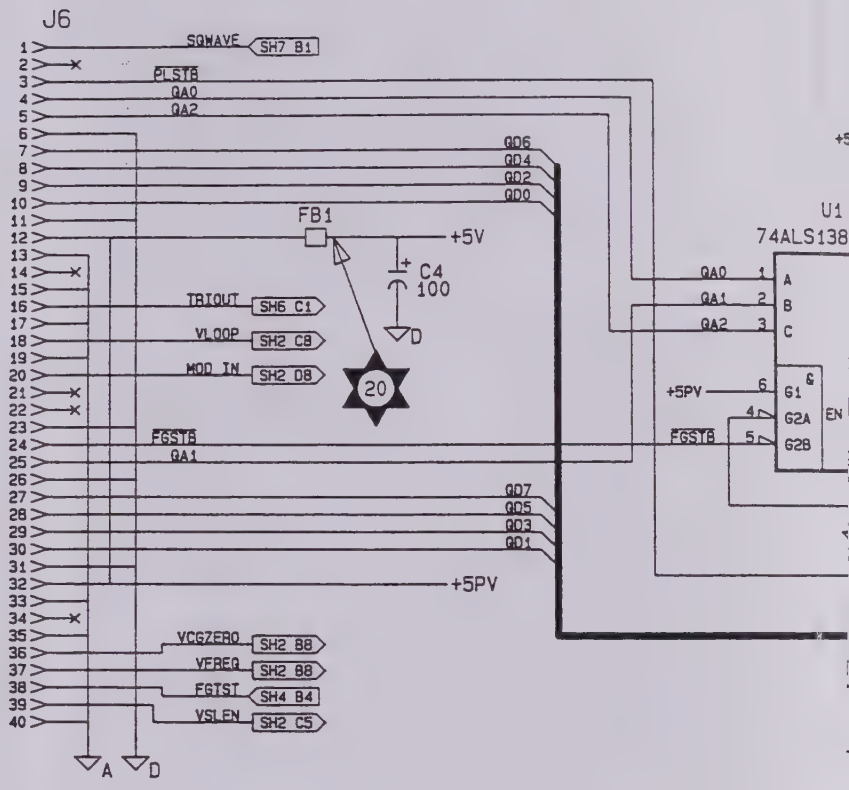
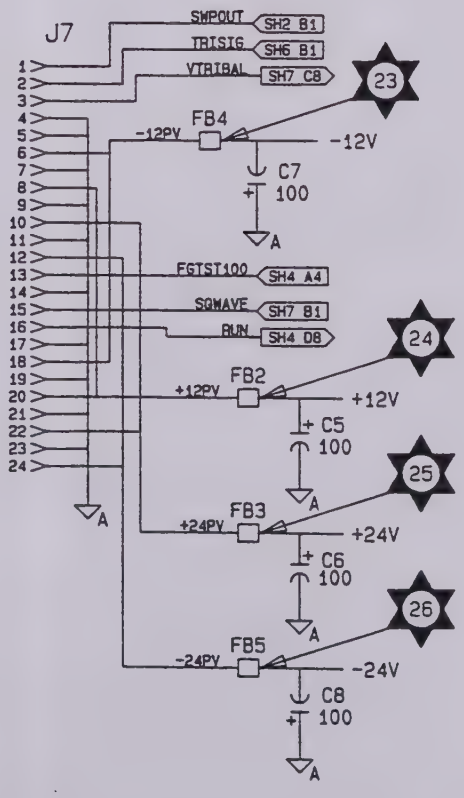
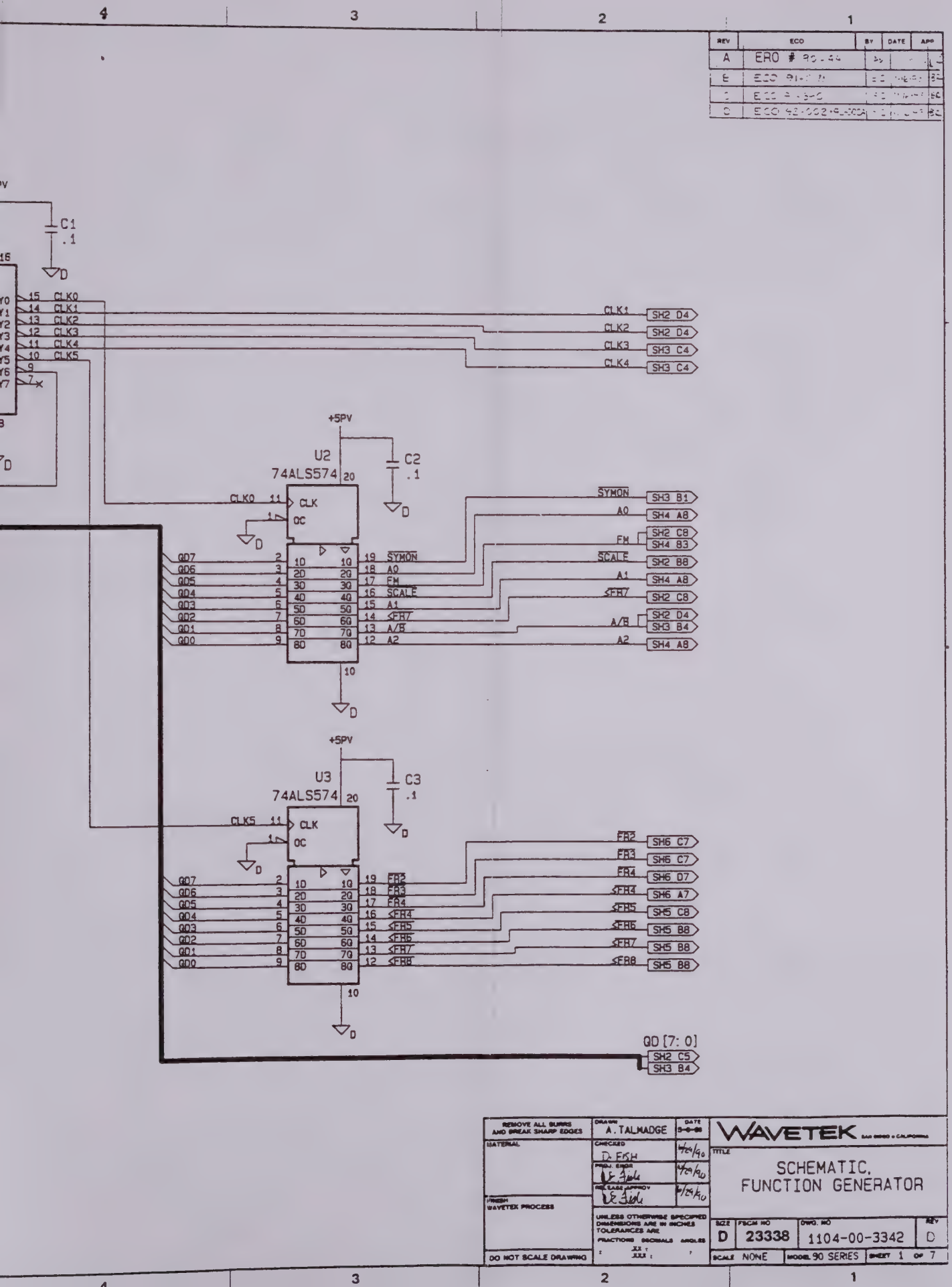



5. TEST POINTS SHOWN AS ✡ ARE FAULT ISOLATION PROCEDURES IN THE UNIT MAINTENANCE MANUAL.
4. ⏚A = ANALOG GROUND SYMBOL.
3. ⏚D = DIGITAL GROUND SYMBOL.
2. ALL CAPACITORS ARE IN MICROFARADS.
1. ALL RESISTORS ARE IN OHMS, 1/8W, 1%, MF.

NOTE UNLESS OTHERWISE SPECIFIED


REV
ECO
BY
DATE
APP
A
ERO # 90-44
B
ECO 91-
C
ECO 91-
D
ECO 92-002
C1
.1
CLK0
CLK1
CLK2
CLK3
CLK4
CLK5
CLK1 SH2 D4
CLK2 SH2 D4
CLK3 SH3 C4
CLK4 SH3 C4
+5PV
U2
74ALS574
C2
.1
CLK
OC
QD7
QD6
QD5
QD4
QD3
QD2
QD1
QD0
SYMON
A0
FM
SCALE
A1
FR7
A/B
A2
SYMON SH3 B1
A0 SH4 A8
FM SH2 C8 SH4 B3
SCALE SH2 B8
A1 SH4 A8
FR7 SH2 C8
A/B SH2 D4 SH3 B4
A2 SH4 A8
U3
74ALS574
C3
.1
FR2
FR3
FR4
FR4
FR5
FR6
FR7
FR8
FR2 SH6 C7
FR3 SH6 C7
FR4 SH6 D7
FR4 SH6 A7
FR5 SH5 C8
FR6 SH5 B8
FR7 SH5 B8
FR8 SH5 B8
QD [7: 0]
SH2 C5
SH3 B4
REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH
WAVETEK PROCESS
DO NOT SCALE DRAWING
DRAWN
A. TALMADGE
DATE
CHECKED
D. FISH
PROJ. ENGR
RELEASE APPROV
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE
FRACTIONS DECIMALS ANGLES
WAVETEK
TITLE
SCHEMATIC,
FUNCTION GENERATOR
SIZE
D
FSCM NO
23338
DWG. NO
1104-00-3342
REV
D
SCALE NONE
MODEL 90 SERIES
SHEET 1 OF 7

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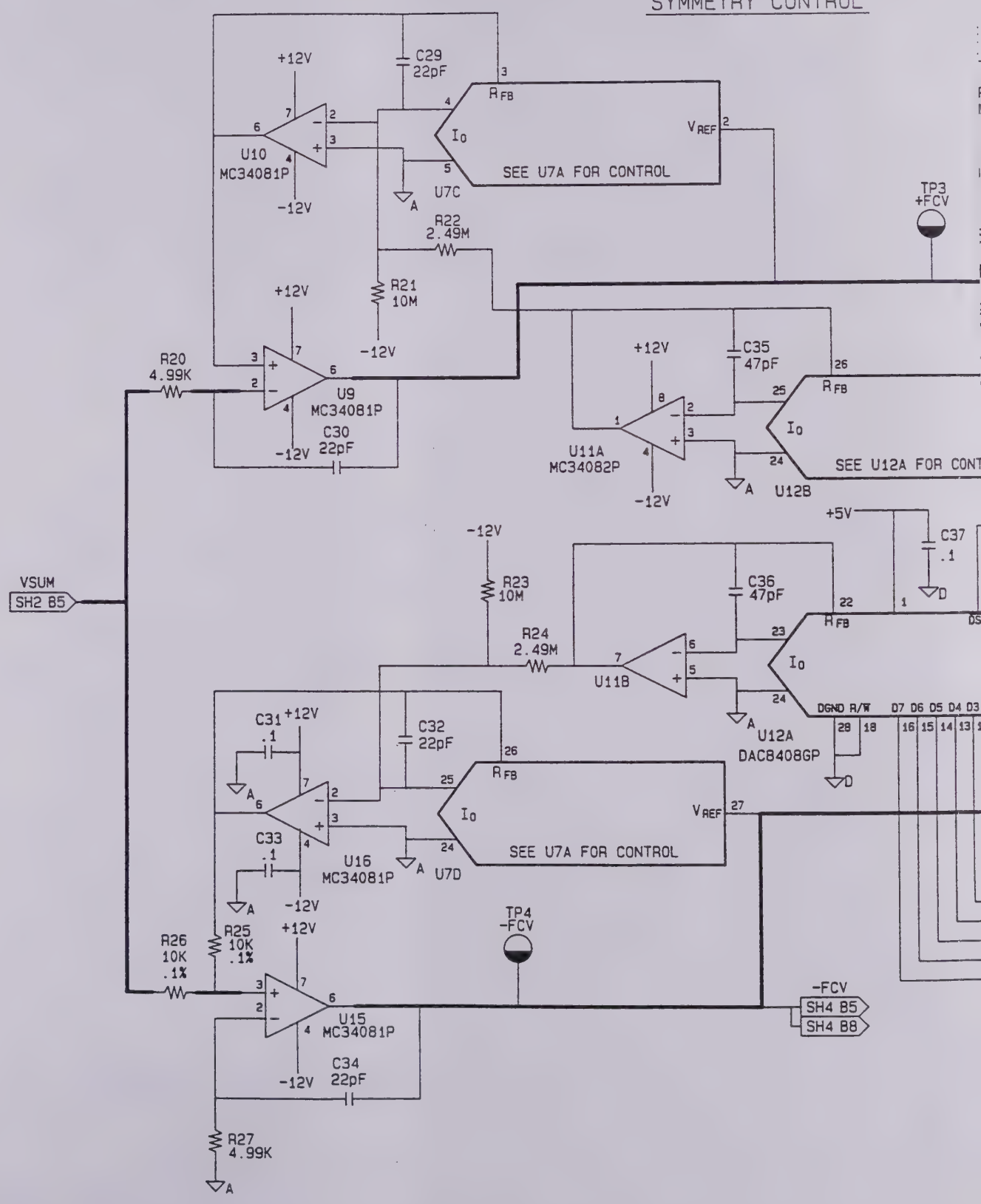
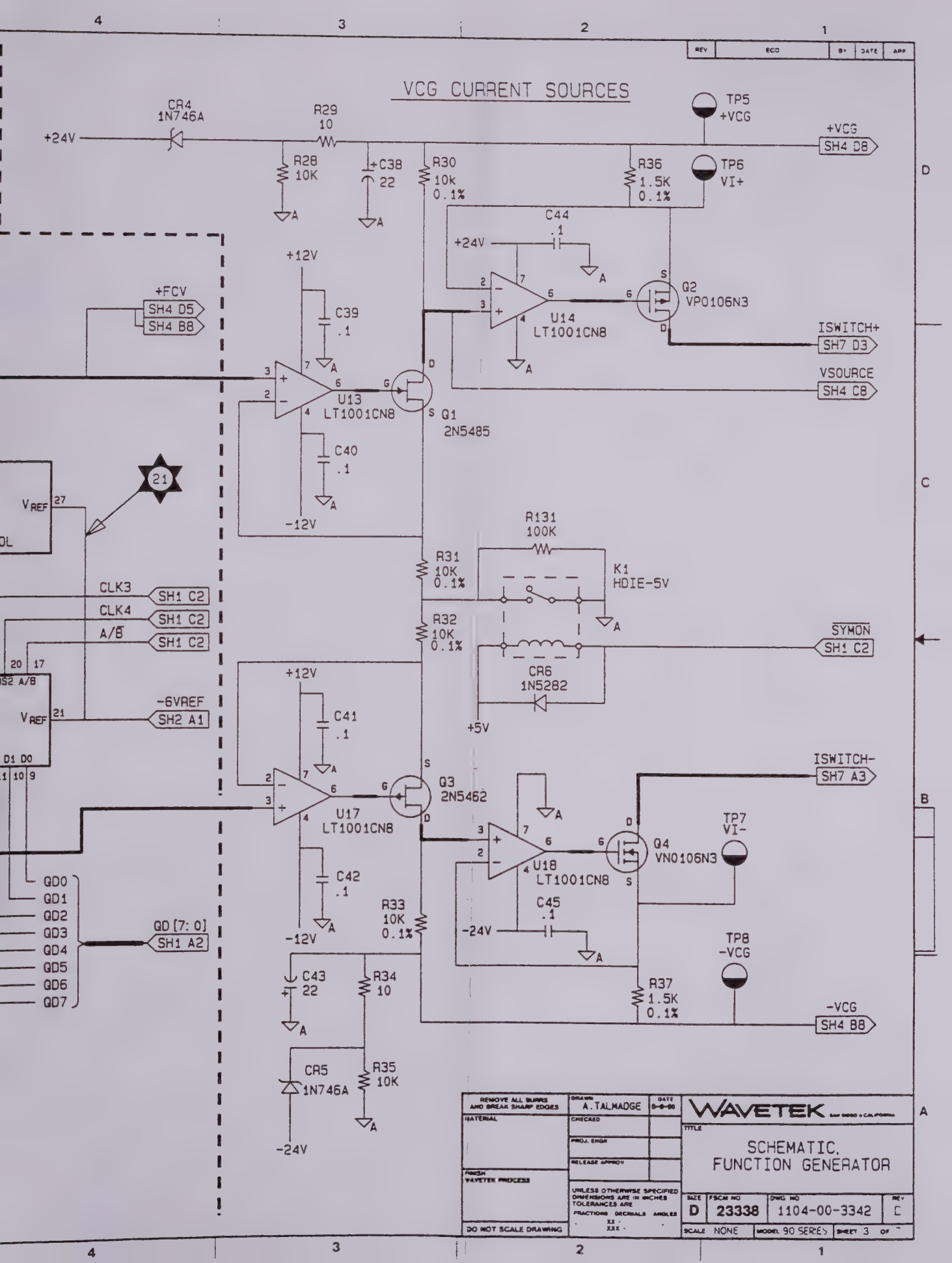
# SYMMETRY CONTROL




NOTE UNLESS OTHERWISE SPECIFIED


VCG CURRENT SOURCES
CR4
1N746A
+24V
R29
10
R28
10K
+C38
22
R30
10k
0.1%
R36
1.5K
0.1%
TP5
+VCG
+VCG
SH4 D8
TP6
VI+
C44
.1
+24V
+12V
+FCV
SH4 D5
SH4 B8
C39
.1
U14
LT1001CN8
Q2
VP0106N3
ISWITCH+
SH7 D3
VSOURCE
SH4 C8
U13
LT1001CN8
Q1
2N5485
C40
.1
-12V
21
VREF
27
R131
100K
R31
10K
0.1%
K1
HDIE-5V
CLK3
SH1 C2
CLK4
SH1 C2
A/B
SH1 C2
R32
10K
0.1%
SYMON
SH1 C2
CR6
1N5282
+5V
-6VREF
SH2 A1
+12V
C41
.1
ISWITCH-
SH7 A3
Q3
2N5462
U17
LT1001CN8
TP7
VI-
Q4
VN0106N3
U18
LT1001CN8
C42
.1
R33
10K
0.1%
C45
.1
-24V
TP8
-VCG
QD0
QD1
QD2
QD3
QD4
QD5
QD6
QD7
QD [7: 0]
SH1 A2
C43
22
R34
10
R37
1.5K
0.1%
-VCG
SH4 B8
CR5
1N746A
R35
10K
-24V
REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH
WAVETEK PROCESS
DRAWN
A. TALMADGE
DATE
CHECKED
PROJ. ENGR
RELEASE APPROV
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE
FRACTIONS DECIMALS ANGLES
DO NOT SCALE DRAWING
WAVETEK
TITLE
SCHEMATIC,
FUNCTION GENERATOR
SIZE
D
FSCM NO
23338
DWG NO
1104-00-3342
REV
C
SCALE NONE
MODEL 90 SERIES
SHEET 3 OF

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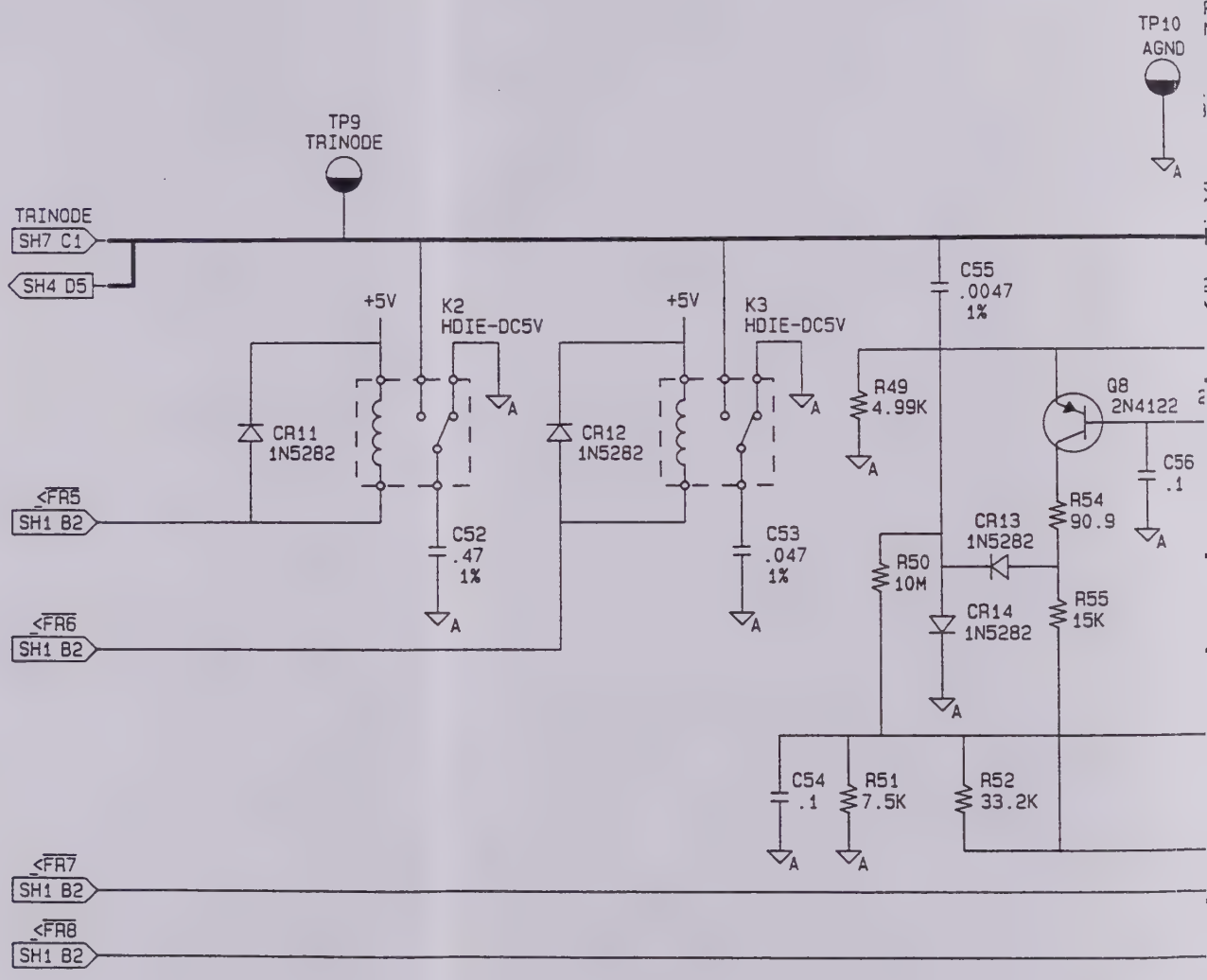
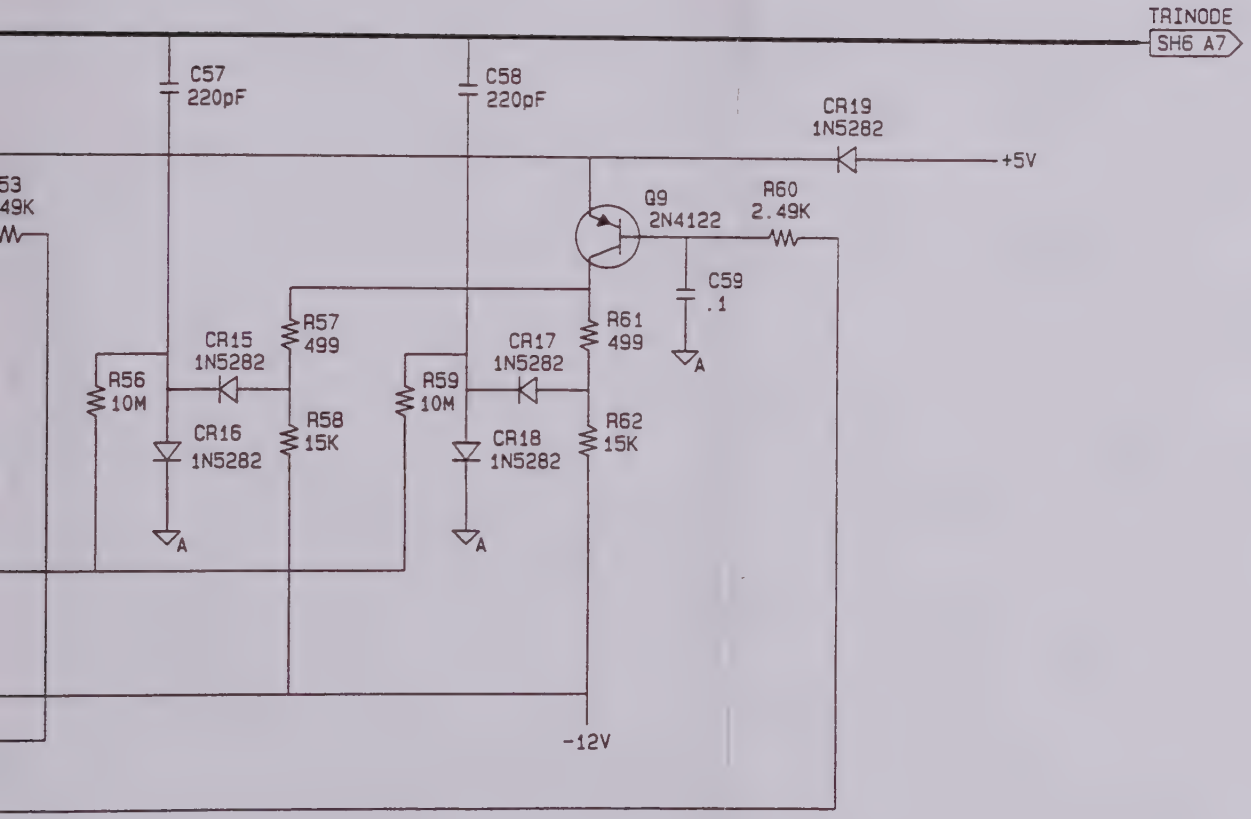
# FREQUENCY RANGE




NOTE UNLESS OTHERWISE SPECIFIED

| REV | ECO | BY | DATE | APP |
|---|---|---|---|---|

## SWITCHES




| | | | |
|---|---|---|---|
| REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN A. TALMADGE | DATE 5-6-80 | WAVETEK SAN DIEGO, CALIFORNIA |
| MATERIAL | CHECKED | | TITLE: SCHEMATIC, FUNCTION GENERATOR |
| | PROJ. ENGR | | |
| FINISH WAVETEK PROCESS | RELEASE APPROV | | |
| DO NOT SCALE DRAWING | UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES .XX ± .XXX ± | | SIZE D · FSCM NO 23338 · DWG NO 1104-00-3342 · REV D · SCALE NONE · MODEL 90 SERIES · SHEET 5 OF 7 |

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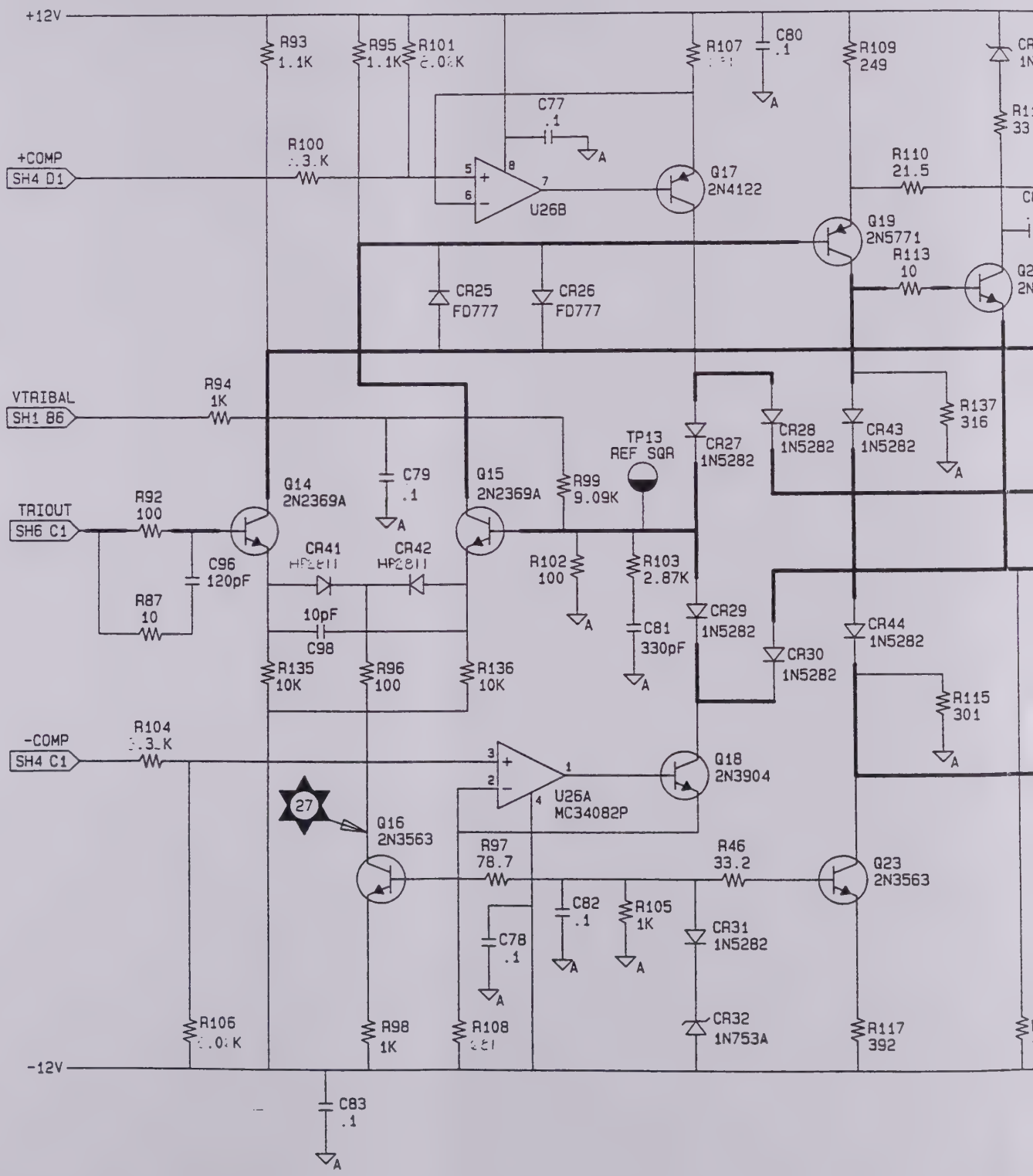
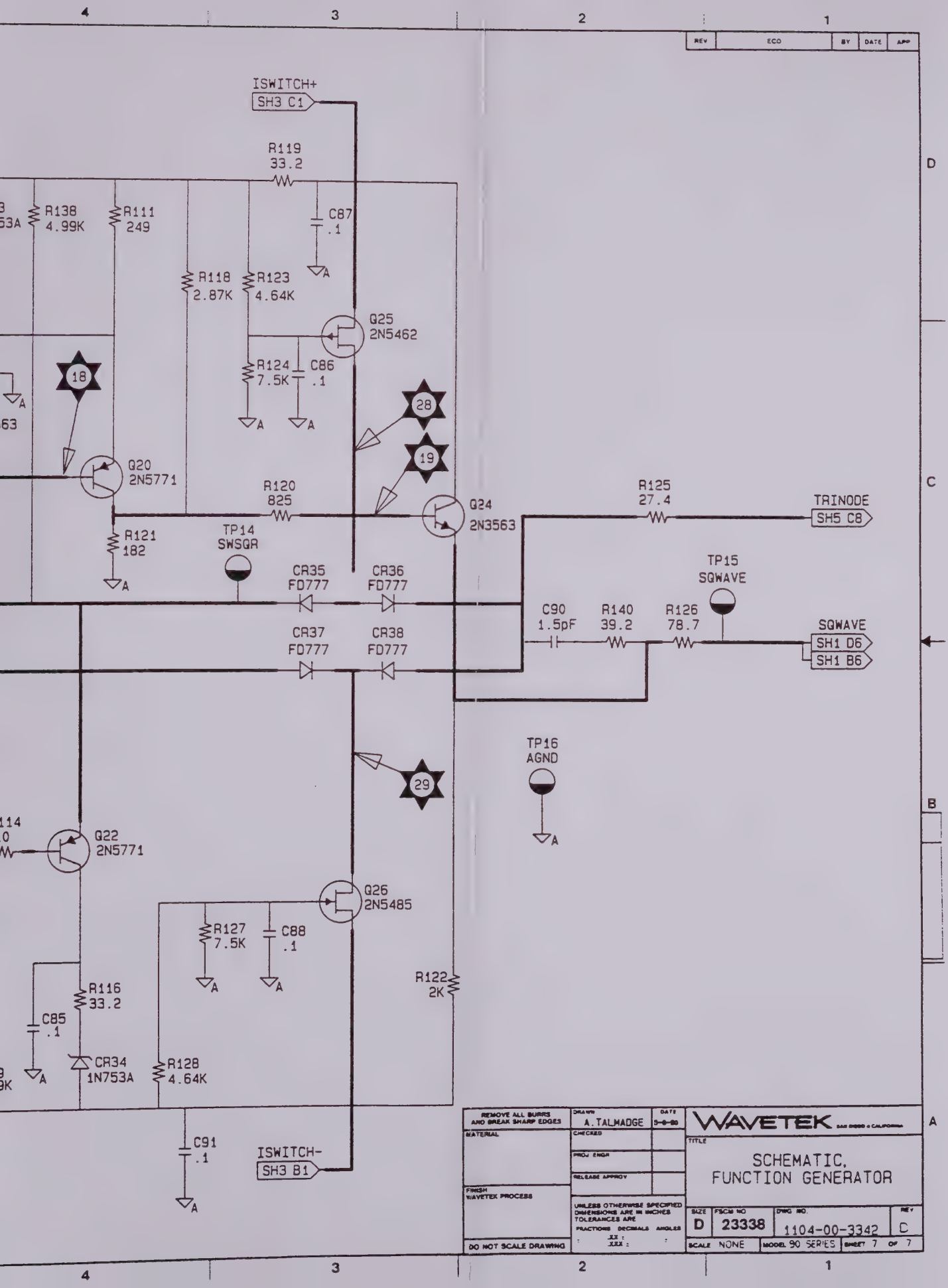
# COMPARATOR




NOTE UNLESS OTHERWISE SPECIFIED


REV
ECO
BY
DATE
APP
ISWITCH+
SH3 C1
R119
33.2
R138
4.99K
R111
249
C87
.1
R118
2.87K
R123
4.64K
Q25
2N5462
R124
7.5K
C86
.1
18
28
19
Q20
2N5771
R120
825
Q24
2N3563
R125
27.4
TRINODE
SH5 C8
R121
182
TP14
SWSQR
CR35
FD777
CR36
FD777
TP15
SQWAVE
C90
1.5pF
R140
39.2
R126
78.7
SQWAVE
SH1 D6
SH1 B6
CR37
FD777
CR38
FD777
TP16
AGND
29
Q22
2N5771
Q26
2N5485
R127
7.5K
C88
.1
R122
2K
R116
33.2
C85
.1
CR34
1N753A
R128
4.64K
C91
.1
ISWITCH-
SH3 B1
REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DO NOT SCALE DRAWING
DRAWN
A. TALMADGE
DATE
CHECKED
PROJ ENGR
RELEASE APPROV
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE
FRACTIONS DECIMALS ANGLES
WAVETEK
TITLE
SCHEMATIC,
FUNCTION GENERATOR
SIZE
D
FSCM NO
23338
DWG NO.
1104-00-3342
REV
C
SCALE NONE
MODEL 90 SERIES
SHEET 7 OF 7

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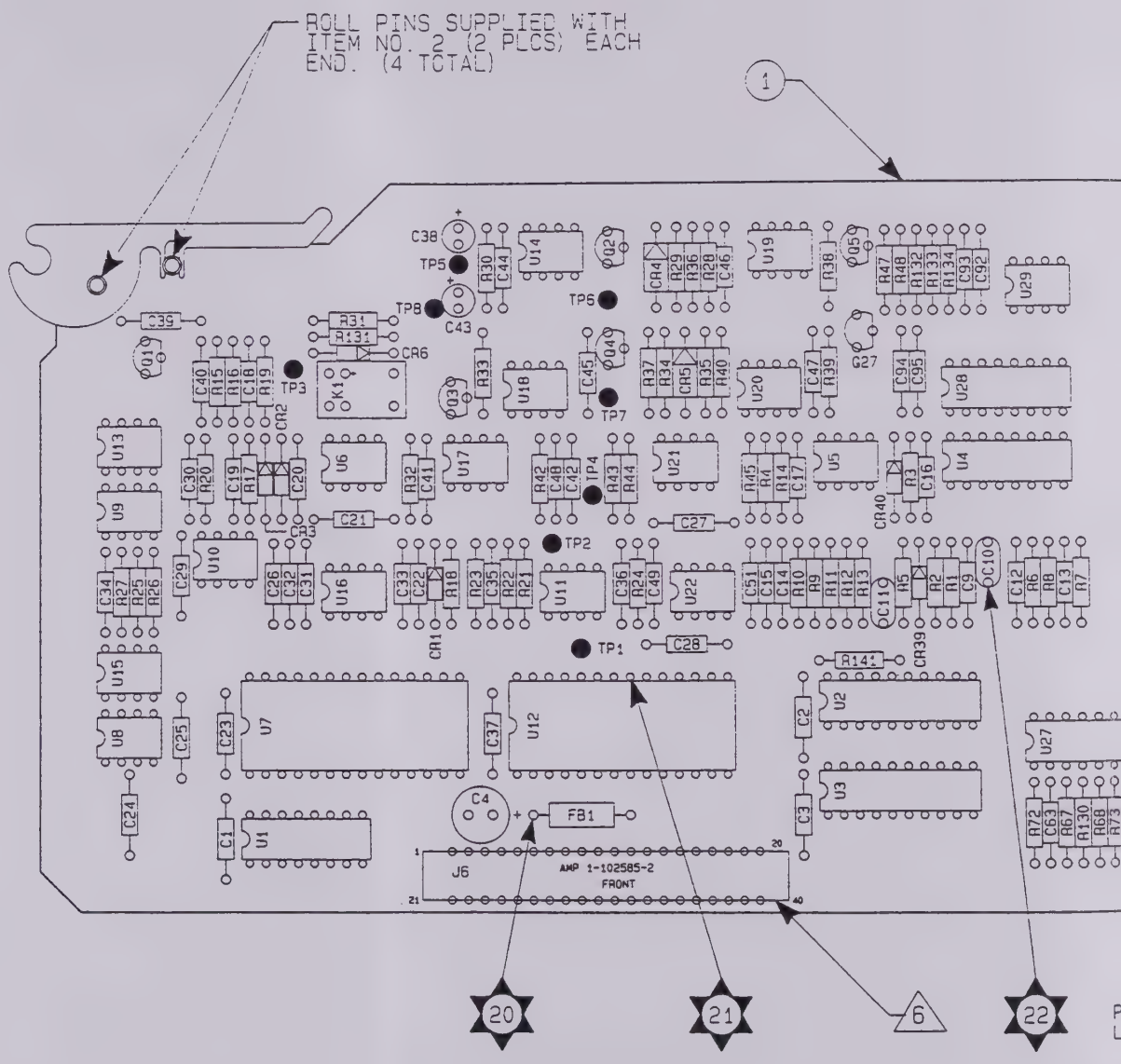
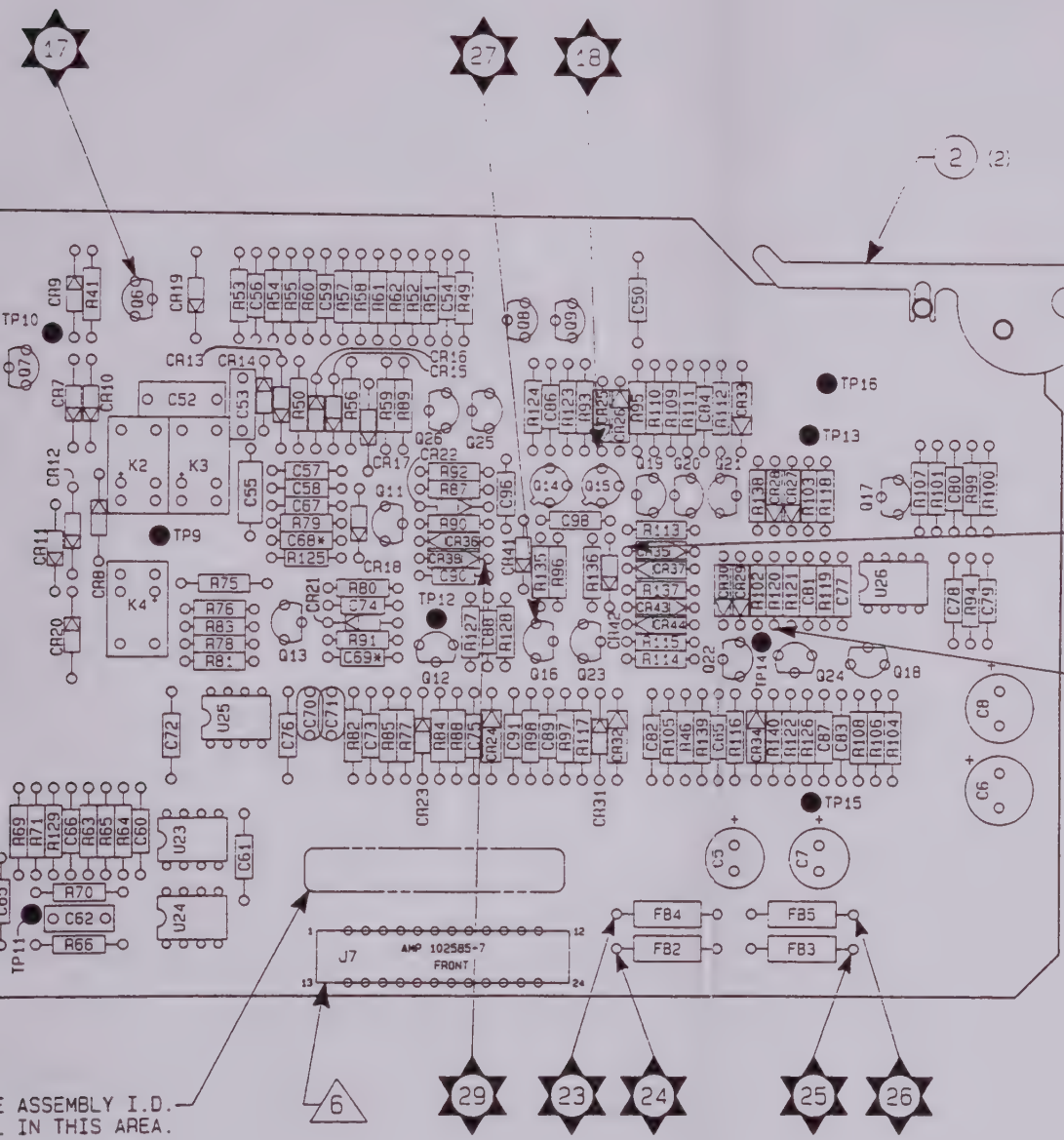



7. TEST POINTS SHOWN AS ✡ ARE FAULT ISOLATION PROCEDURES IN THE UNIT MAINTENANCE MANUAL.
6. MANUFACTURER'S MARKING INDICATES CORRECT ORIENTATION OF CONNECTOR.
5. * = TRIM.
4. ASSEMBLE PER WAVETEK WORKMANSHIP STANDARDS.
3. REFERENCE DESIGNATIONS DO NOT APPEAR ON PARTS.
2. FOR ASSEMBLY INTERCONNECTION, SEE INSTRUMENT SCHEMATIC.
1. SEE 1104-00-3342 FOR SCHEMATIC.

NOTE UNLESS OTHERWISE SPECIFIED

| REV | ECO | BY | DATE | APP |
|---|---|---|---|---|
| 4 | [illegible] | AV | [illegible] | [illegible] |
| 5 | ECO [illegible] | T | [illegible] | [illegible] |




E ASSEMBLY I.D.
IN THIS AREA.

CAD JOB #: B065C

| | | | |
|---|---|---|---|
| REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN: Amy Talmadge | DATE: 6-20-90 | WAVETEK |
| MATERIAL | CHECKED | | TITLE: PCA, FUNCTION GENERATOR BOARD |
| | PROJ ENGR | 7/24/90 | |
| FINISH: WAVETEK PROCESS | RELEASE APPROV | 7/24/90 | |
| DO NOT SCALE DRAWING | UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ± .XXX ± | | SIZE: D; FSCM NO: 23338; DWG NO: 1101-00-3342; REV: B; SCALE: 2/1; MODEL: 90 SERIES; SHEET: 1 OF 1 |

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

| REFERENCE DESIGNATORS | PART DESCRIPTION | ORIG-MFGR-PART-NO | MFGR | WAVETEK NO. | QTY/PT |
|---|---|---|---|---|---|
| REF | MODEL 90 SUB-ASY FUNCTION TEST PROCESS | 1008-00-0596-1 | WVTK | 1008-00-0596-1 | 1 |
| NONA | A/D, PCA, FUNCTION GENERATOR | 1101-00-3342 | WVTK | 1101-00-3342 | 1 |
| NONE | S/D, PCA, FUNCTION GENERATOR | 1104-00-3342 | WVTK | 1104-00-3342 | 1 |
| CR1 CR24 CR32 CR33 CR34 | SL ZR 6 2V 5% 400MW (1N753A) | 1N753A | ROHM | 131.9620 | 5 |
| C98 | CAP CER 10PF 200V 5% AXIAL | CAC02C0G100J100A(OBS) | CORNG | 1500-01-0006 | 1 |
| C17 | CAP, CER, 100PF, 100V, AXIAL | CAC02C0G101J100A(OBS) | CORNG | 1500-01-0106 | 1 |
| C1 C12 C13 C14 C15 C16 C18 C2 C20 C21 C22 C23 C25 C27 C28 C3 C31 C33 C37 C39 C40 C41 C42 C44 C45 C46 C47 C48 C50 C54 C56 C59 C60 C61 C63 C64 C65 C72 C73 C74 C75 C76 C77 C78 C79 C80 C82 C83 C84 C85 C86 C87 C88 C9 C91 C92 C93 C94 C95 | CAP, CER, MON, .1MF, 50V, AXIAL | CAC03Z5U104Z030A | CORNG | 1500-01-0405 | 59 |
| C96 | CAP, CER, 120PF 200V 5% AXIAL | SA102A121JAA | AVX | 1500-01-2106 | 1 |
| C67 | CAP, CER, 15PF, 100V, AXIAL | CAC02C0G150J100A | CORNG | 1500-01-3006 | 1 |

| WAVETEK PARTS LIST | TITLE: PCA, FUNCTION GENERATOR | ASSEMBLY NO. 1100-00-3342 | REV F |
|---|---|---|---|

PAGE 1

| REFERENCE DESIGNATORS | PART DESCRIPTION |
|---|---|
| | DIAL |
| C53 C62 | CAP, MYLR, .047MF, 50V |
| C52 | CAP, MYLR, .47MF, 50V |
| NONE | PCB, FUNCTION GENERATOR BD REF. SPEC 0008-00-0455 REV E |
| J7 | CONN, HEADER, 24 PIN, RECPT, 2X12, .1 CTR, PCMT |
| J6 | CONN, HEADER, 40 PIN, RECPT, 2X20, .1 CTR PCMT |
| TP1 TP10 TP16 | TEST POINT, BLK, PC |
| TP11 TP12 TP13 TP14 TP15 TP2 TP3 TP4 TP5 TP6 TP7 TP8 TP9 | TEST POINT, RED, PC |
| NONE | PC BD EJECTOR |
| FB1 FB2 FB3 FB4 FB5 | BALUN CORE, FERRITE, 680 OHMS |
| K1 K2 K3 K4 | RELAY, 1 FORMC, 5V, .312H, .296W |

| WAVETEK PARTS LIST | TITLE: PCA, FUNCTION GENERATOR |
|---|---|

| REFERENCE DESIGNATORS | PART DESCRIPTION | ORIG-MFGR-PART-NO | MFGR | WAVETEK NO. | QTY/PT |
|---|---|---|---|---|---|
| C90 | CAP, CER, 1.5PF, 200V, AXIAL | SA102A1R5DAA | AVX | 1500-01-5906 | 1 |
| C29 C30 C32 C34 | CAP, CER, 22PF, 100V, AXIAL | CAC02C0G220J100A(OBS) | CORNG | 1500-02-2006 | 4 |
| C57 C58 | CAP, CER, 220PF, 100V, AXIAL | CAC02C0G221J100A | CORNG | 1500-02-2106 | 2 |
| C10 C70 C71 | CAP, CER, .22MF, 25V | CW30C224K | CRL | 1500-02-2409 | 3 |
| C19 C81 | CAP, CER, 330PF, 100V, AXIAL | CAC02C0G331J100A | CORNG | 1500-03-3106 | 2 |
| C11 C66 | CAP, CER, 3300PF, 100V, 2 OZ, AXIAL | CAC02X7R332M100A(OBS) | CORNG | 1500-03-3206 | 2 |
| C35 C36 C49 C51 | CAP CER 47PF 200V 5% AXIAL | CAC02C0G470J100A(OBS) | CORNG | 1500-04-7006 | 4 |
| C55 | CAP, CER, 4700PF, 50V, 2% | 592CC0G472G050E | SPRAG | 1500-04-7213 | 1 |
| C24 C26 | CAP, CER, 680PF, 100V, AXIAL | CAC02C0G681J100A | CORNG | 1500-06-8106 | 2 |
| C6 C8 | CAP, ELECT, 100MF, 35V RADIAL LEAD, SP .20 | NRE101M35V10X12.5(OBS) | NIC | 1500-31-0102 | 2 |
| C4 C5 C7 | CAP, ELECT, 100MF, 25V, RADIAL LEAD-SP SIZE | NRE101M25V6.3X11 | NIC | 1500-31-0122 | 3 |
| C38 C43 | CAP, ELECT, 22MF, 25V, RA | SRA25V822RM6X7LL | UNCON | 1500-32-2002 | 2 |

| WAVETEK PARTS LIST | TITLE: PCA, FUNCTION GENERATOR | ASSEMBLY NO. 1100-00-3342 | REV F |
|---|---|---|---|

PAGE 2

| REFERENCE DESIGNATORS | PART DESCRIPTION |
|---|---|
| R25 R26 R30 R31 R32 R33 R67 | RES, MF, 1/8W, .1%, 10K |
| R68 | RES, MF, 1/8W, .1%, 100K |
| R69 | RES, MFLM, 1/8W, 0.1%, 1.0M |
| R36 R37 | RES, MF, 1/8W, .1%, 1.5K |
| R102 R65 R83 R92 R96 | RES, MF, 1/8W, 1%, 100 |
| R103 R64 R85 R94 R98 | RES, MF, 1/8W, 1%, 1K |
| R135 R136 R28 R3 R35 R38 R39 R41 R47 R5 | RES, MF, 1/8W, 1%, 10K |
| R11 R12 R131 R48 R76 | RES, MF, 1/8W, 1%, 100K |
| R78 | RES, MF, 1/8W, 1%, 1M |
| R21 R23 R50 R56 R59 R71 R75 | RES, MF, 1/4W, 10M, 1% |
| R113 R114 R29 R34 R66 R70 R79 R87 R90 | RES, MF, 1/8W, 1%, 10 |
| R93 R95 | RES, MF, 1/8W, 1%, 1.1K |
| R141 | RES, MF, 1/8W, 1%, 11K |
| R55 R58 R62 | RES, MF, 1/8W, 1%, 15K |
| R121 R89 | RES, MF, 1/8W, 1%, 182 |

| WAVETEK PARTS LIST | TITLE: PCA, FUNCTION GENERATOR |
|---|---|

NOTE UNLESS OTHERWISE SPECIFIED

8 7 6 5

| REV | ECO | BY | DATE | APP |
|---|---|---|---|---|

| ORIG-MFGR-PART-NO | MFGR | WAVETEK NO | QTY/PT |
|---|---|---|---|
| 5R473F | ELPAC | 1300-44-7303 | 2 |
| 5R474F | ELPAC | 1300-44-7403 | 1 |
| 700-00-3342 | WVTK | 1700-00-3342 | 1 |
| -0102584-7(REF ONLY) | AMP | 2100-02-0255 | 1 |
| -0102585-2(REF ONLY) | AMP | 2100-02-0256 | 1 |
| P-104-01-00 | COMPO | 2100-04-0054 | 3 |
| P-104-01-02 | COMPO | 2100-04-0055 | 13 |
| 7-2-C | BRIT | 2800-07-0032 | 2 |
| 943666671 | FARIT | 3100-00-0017 | 3 |
| D1E-M-DC5V | AROMT | 4500-00-0034 | 4 |

| ASSEMBLY NO. | REV |
|---|---|
| 1100-00-3342 | F |



| REFERENCE DESIGNATORS | PART DESCRIPTION | ORIG-MFGR-PART-NO | MFGR | WAVETEK NO | QTY/PT |
|---|---|---|---|---|---|
| R122 | RES. MF. 1/8W. 1%. 2K | RN55D-2001F | TRW | 4701-03-2001 | 1 |
| R42 R44 | RES. MF. 1/8W. 1%. 20K | RN55D-2002F | TRW | 4701-03-2002 | 2 |
| R110 | RES. MF. 1/8W. 1%. 21. 5 | RN55D-21R5F | TRW | 4701-03-2159 | 1 |
| R109 R111 | RES. MF. 1/8W. 1%. 249 | RN55D-2490F | TRW | 4701-03-2490 | 2 |
| R1 R13 R2 R53 R6 R60 R7 R72 R73 R74 | RES. MF. 1/8W. 1%. 2 49K | RN55D-2491F | TRW | 4701-03-2491 | 10 |
| R130 R22 R24 | RES. MFLM. 1/8W. 2. 49M. 1 % | CMF-552494F T-8 | DALE | 4701-03-2494 | 3 |
| R125 | RES. MF. 1/8W. 1%. 27. 4 | RN55D-27R4F | TRW | 4701-03-2749 | 1 |
| R103 R118 | RES. MF. 1/8W. 1%. 2. 87K | RN55D-2871F | TRW | 4701-03-2871 | 2 |
| R115 | RES. MF. 1/8W. 1%. 301 | RN55D-3010F | TRW | 4701-03-3010 | 1 |
| R43 R45 | RES. MF. 1/8W. 1%. 30. 1K | RN55D-3012F | TRW | 4701-03-3012 | 2 |
| R137 | RES. MF. 1/8W. 1%. 316 | RN55D-3160F | TRW | 4701-03-3160 | 1 |
| R84 | RES. MF. 1/8W. 1%. 3. 24K | RN55D-3241F | TRW | 4701-03-3241 | 1 |
| R100 R104 | RES. MF. 1/8W. 1%. 3. 32K | RN55D-3321F | TRW | 4701-03-3321 | 2 |
| R52 | RES. MF. 1/8W. 1%. 30. 2K | RN55D-3322F | TRW | 4701-03-3322 | 1 |
| R112 R116 R119 R46 | RES. MF. 1/8W. 1%. 33. 2 | RN55D-33R2F | TRW | 4701-03-3329 | 4 |
| R117 | RES. MF. 1/8W. 1%. 392 | RN55D-3920F | TRW | 4701-03-3920 | 1 |

| WAVETEK PARTS LIST | TITLE | ASSEMBLY NO. | REV |
|---|---|---|---|
| | PCA. FUNCTION GENERATOR | 1100-00-3342 | F |



| RIG-MFGR-PART-NO | MFGR | WAVETEK NO. | QTY/PT |
|---|---|---|---|
| N55E-1002B | MEPCO | 4701-02-1002 | 7 |
| N55E-1003B | MEPCO | 4701-02-1003 | 1 |
| MF-55-1004BT-9 | DALE | 4701-02-1004 | 1 |
| N55E-1501B | CORNG | 4701-02-1501 | 2 |
| N55D-1000F | TRW | 4701-03-1000 | 3 |
| N55D-1001F | TRW | 4701-03-1001 | 5 |
| N55D-1002F | TRW | 4701-03-1002 | 10 |
| N55D-1003F | TRW | 4701-03-1003 | 5 |
| N55D-1004F | TRW | 4701-03-1004 | 1 |
| 053YD10M000F | MEPCO | 4701-03-1005 | 7 |
| 043ED10R100F | MEPCO | 4701-03-1009 | 9 |
| N55D-1101F | TRW | 4701-03-1101 | 2 |
| N55D-1102F | TRW | 4701-03-1102 | 1 |
| N55D-1302F | TRW | 4701-03-1302 | 3 |
| N55D-1820F | TRW | 4701-03-1820 | 2 |

| ASSEMBLY NO. | REV |
|---|---|
| 1100-00-3342 | F |



| REFERENCE DESIGNATORS | PART DESCRIPTION | ORIG-MFGR-PART-NO | MFGR | WAVETEK NO. | QTY/PT |
|---|---|---|---|---|---|
| R140 | RES. MF. 1/8W. 1%. 39. 2 | RN55D-39R2F | TRW | 4701-03-3929 | 1 |
| R10 R14 R9 | RES. MF. 1/8W. 1%. 4. 02K | RN55D-4021F | TRW | 4701-03-4021 | 3 |
| R123 R128 | RES. MF. 1/8W. 1%. 4. 64K | RN55D-4641F | TRW | 4701-03-4641 | 2 |
| R129 R18 R57 R61 | RES. MF. 1/8. 1%. 499 | RN55D-4990F | TRW | 4701-03-4990 | 4 |
| R134 R138 R139 R20 R27 R49 R63 R82 | RES. MF. 1/8W. 1%. 4. 99K | RN55D-4991F | TRW | 4701-03-4991 | 8 |
| R132 R17 | RES. MF. 1/8W. 1%. 49. 9K | RN55D-4992F | TRW | 4701-03-4992 | 2 |
| R133 | RES. MF. 1/8W. 1%. 499K | RN55D-4993F | TRW | 4701-03-4993 | 1 |
| R80 R91 | RES. MF. 1/8W. 1%. 51. 1 | RN55D-51R1F | TRW | 4701-03-5119 | 2 |
| R19 | RES. MF. 1/8W. 1%. 604 | RN55D-6040F | TRW | 4701-03-6040 | 1 |
| R107 R108 | RES. MF. 1/8W. 1%. 681 | RN55D-6810F | TRW | 4701-03-6810 | 2 |
| R40 | RES. MF. 1/8W. 1%. 730 | RN55D-7300F | TRW | 4701-03-7300 | 1 |
| R124 R127 R16 R51 | RES. MF. 1/8W. 1%. 7. 5K | RN55D-7501F | TRW | 4701-03-7501 | 4 |
| R81 | RES. MF. 1/8W. 1%. 78. 7K | RN55D-7872F | TRW | 4701-03-7872 | 1 |
| R126 R97 | RES. MF. 1/8W. 1%. 78. 7 | RN55D-78R7F | TRW | 4701-03-7879 | 2 |
| R101 R106 R4 | RES. MF. 1/8W. 1%. 8. 06K | RN55D-8061F | TRW | 4701-03-8061 | 3 |
| R120 | RES. MF. 1/8W. 1%. 825 | RN55D-8250F | TRW | 4701-03-8250 | 1 |

| WAVETEK PARTS LIST | TITLE | ASSEMBLY NO. | REV |
|---|---|---|---|
| | PCA. FUNCTION GENERATOR | 1100-00-3342 | F |



| REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN | DATE |
|---|---|---|
| MATERIAL | CHECKED | |
| | PROJ. ENGR | |
| | RELEASE APPROV | |
| FINISH WAVETEK PROCESS | UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES .XX ± .XXX ± | |
| DO NOT SCALE DRAWING | | |

WAVETEK San Diego, California

TITLE

PARTS LIST
FUNCTION GENERATOR BD.

| SIZE | FSCM NO | DWG. NO | REV |
|---|---|---|---|
| D | 23338 | 1100-00-3342 | F |

| SCALE | MODEL | SHEET |
|---|---|---|
| | 90 | 1 OF 2 |

4 3 2 1

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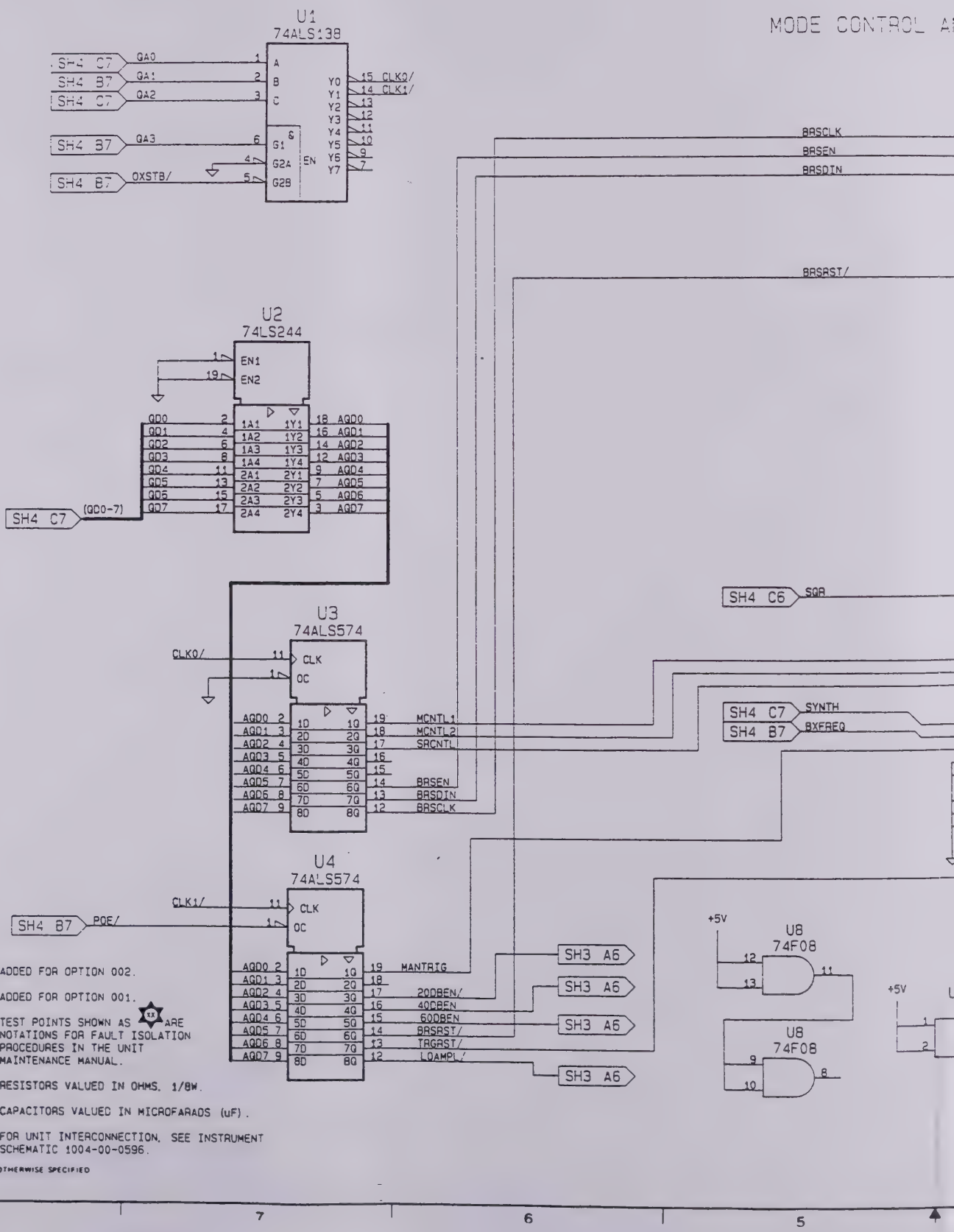
# CONTROL I/O




6. ADDED FOR OPTION 002.

5. ADDED FOR OPTION 001.

4. TEST POINTS SHOWN AS XX ARE NOTATIONS FOR FAULT ISOLATION PROCEDURES IN THE UNIT MAINTENANCE MANUAL.

3. RESISTORS VALUED IN OHMS, 1/8W.

2. CAPACITORS VALUED IN MICROFARADS (uF).

1. FOR UNIT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 1004-00-0596.

NOTE UNLESS OTHERWISE SPECIFIED

| REV | ECO | BY | DATE | APP |
|---|---|---|---|---|
| B | ECO 91-02 | | | |

# BURST COUNTER

U5
DNC2016

SCLK 1
SEN 2
SDIN 3
SLDA 5
ALDA 7
SLDB 10
ALDB 11
MRES 8
TMEN 21
CLKA 4
CLKS 9
PLD 22
OSCOUT 12
SDOUT 13
CYA 20
CYDA 19
CYB 16
CYDB 15

U8/B
74F08
4
5
6

R3
90.9
+5V

SQWAVE
SH4 C7

TP1
TP2
TP3

RUN
SH4 C6

BRCP
BURST

U6
GL20V8
I1/CLK 1
I2 2
I3 3
I4 4
I5 5
I6 6
I7 7
I8 8
I9 9
I10 10
I11 11
I12 23
I13 14
I14/OE 13
Q1 22
Q2 21
Q3 20
Q4 19
Q5 18
Q6 17
Q7 16
Q8 15

BSET
JSET
KSET

U7/A
74F112
SET 4
J 3
CLK 1
K 2
CLR 15
Q 5
Q̄ 6

QNOT

+5V

U7
74F112
SET 10
J 11
CLK 13
K 12
CLR 14
Q 9
Q̄ 7

74F08
3

CAD JOB #: 8059 B

| | | | |
|---|---|---|---|
| REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN | GENE M | 5/22/90 |
| MATERIAL | CHECKED | L ASH | 5/29/90 |
| | PROJ ENGR | [illegible] | 5/29/90 |
| | RELEASE APPROV | [illegible] | 5/29/90 |
| FINISH WAVETEK PROCESS | UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES .XX ± .XXX ± | | |
| DO NOT SCALE DRAWING | | | |

WAVETEK SAN DIEGO, CALIFORNIA

TITLE
SCHEMATIC,
AUX BOARD

| SIZE | FSCM NO | DWG NO | REV |
|---|---|---|---|
| D | 23338 | 1104-00-3386 | B |

SCALE N/A MODEL 90 SHEET 2 OF 4

1104-00-3386 B

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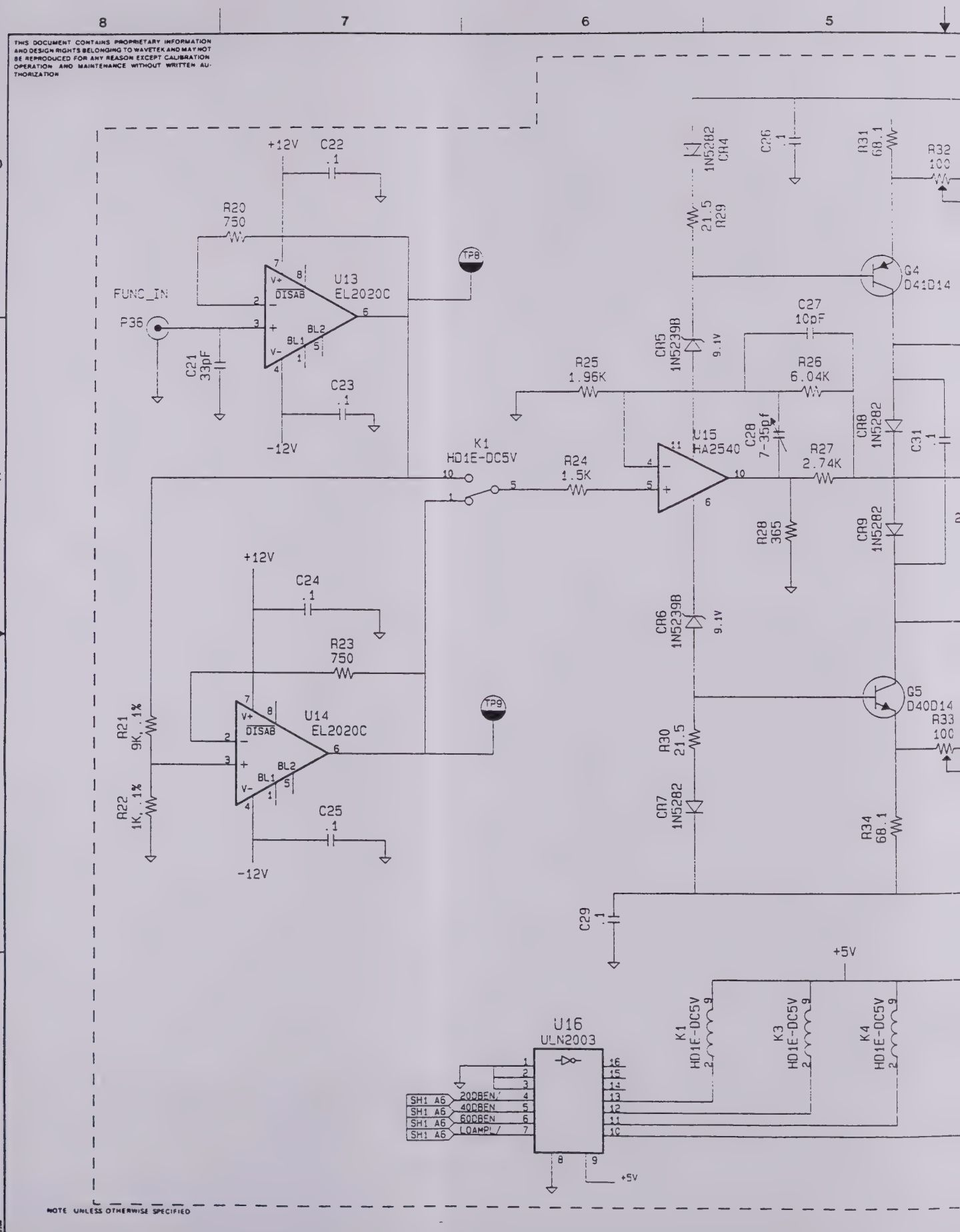
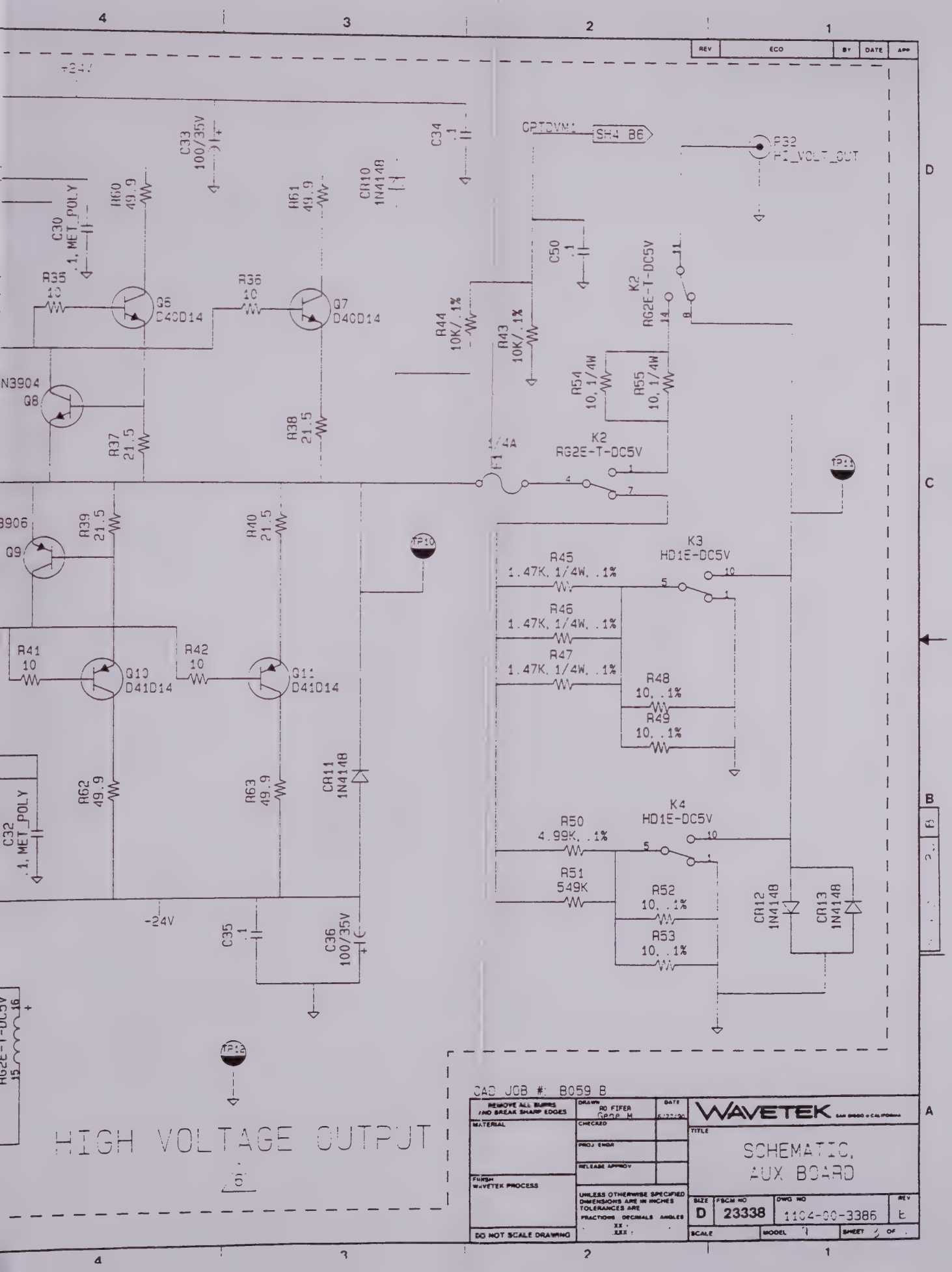



NOTE UNLESS OTHERWISE SPECIFIED


REV
ECO
BY
DATE
APP
C33
100/35V
C34
.1
CR10
1N4148
C30
.1, MET_POLY
R60
49.9
R61
49.9
R35
10
R36
10
Q6
D40D14
Q7
D40D14
OPTOVM
SH4 B6
P32
FI_VOLT_OUT
C50
.1
K2
RG2E-T-DC5V
R44
10K/.1%
R43
10K/.1%
R54
10, 1/4W
R55
10, 1/4W
N3904
Q8
R37
21.5
R38
21.5
1/4A
F1
K2
RG2E-T-DC5V
TP11
3906
Q9
R39
21.5
R40
21.5
TP10
K3
HD1E-DC5V
R45
1.47K, 1/4W, .1%
R46
1.47K, 1/4W, .1%
R47
1.47K, 1/4W, .1%
R48
10, .1%
R49
10, .1%
R41
10
R42
10
Q10
D41D14
Q11
D41D14
C32
.1, MET_POLY
R62
49.9
R63
49.9
CR11
1N4148
K4
HD1E-DC5V
R50
4.99K, .1%
R51
549K
R52
10, .1%
R53
10, .1%
CR12
1N4148
CR13
1N4148
-24V
C35
.1
C36
100/35V
TP12
HIGH VOLTAGE OUTPUT
CAD JOB #: B059 B
REMOVE ALL BURRS AND BREAK SHARP EDGES
DRAWN
RO FIFER
Gene M
DATE
6/27/90
CHECKED
PROJ ENGR
RELEASE APPROV
MATERIAL
FINISH
WAVETEK PROCESS
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE
FRACTIONS DECIMALS ANGLES
XX
XXX
DO NOT SCALE DRAWING
WAVETEK SAN DIEGO, CALIFORNIA
TITLE
SCHEMATIC,
AUX BOARD
SIZE
D
FSCM NO
23338
DWG NO
1104-00-3386
REV
E
SCALE
MODEL
SHEET
OF

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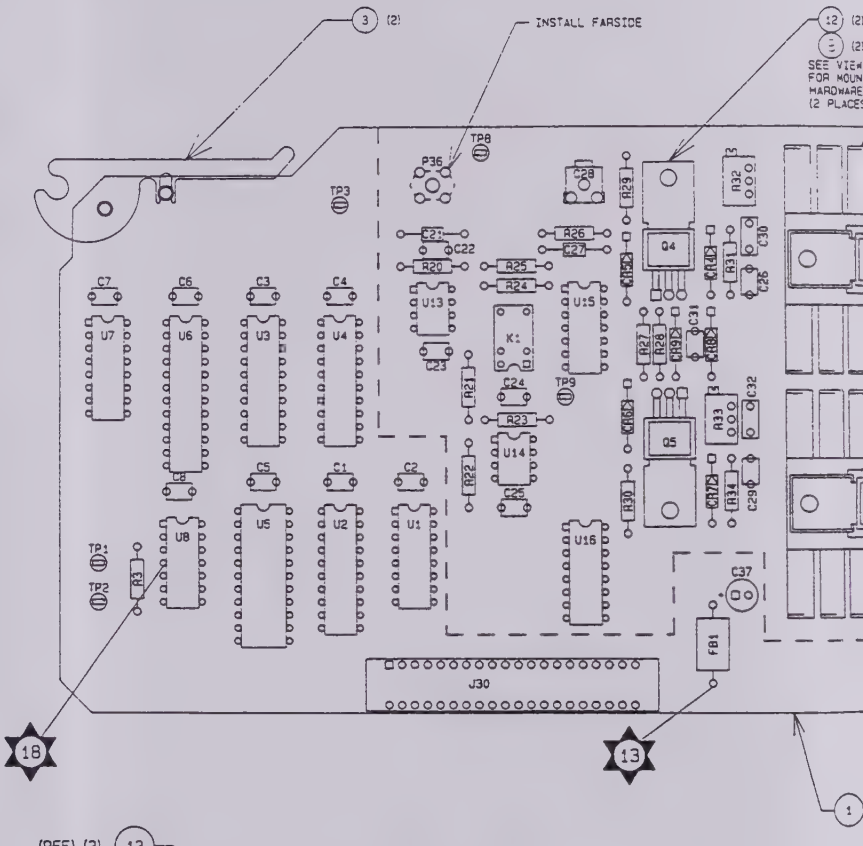
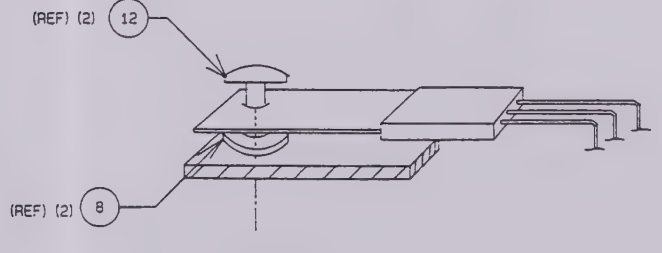


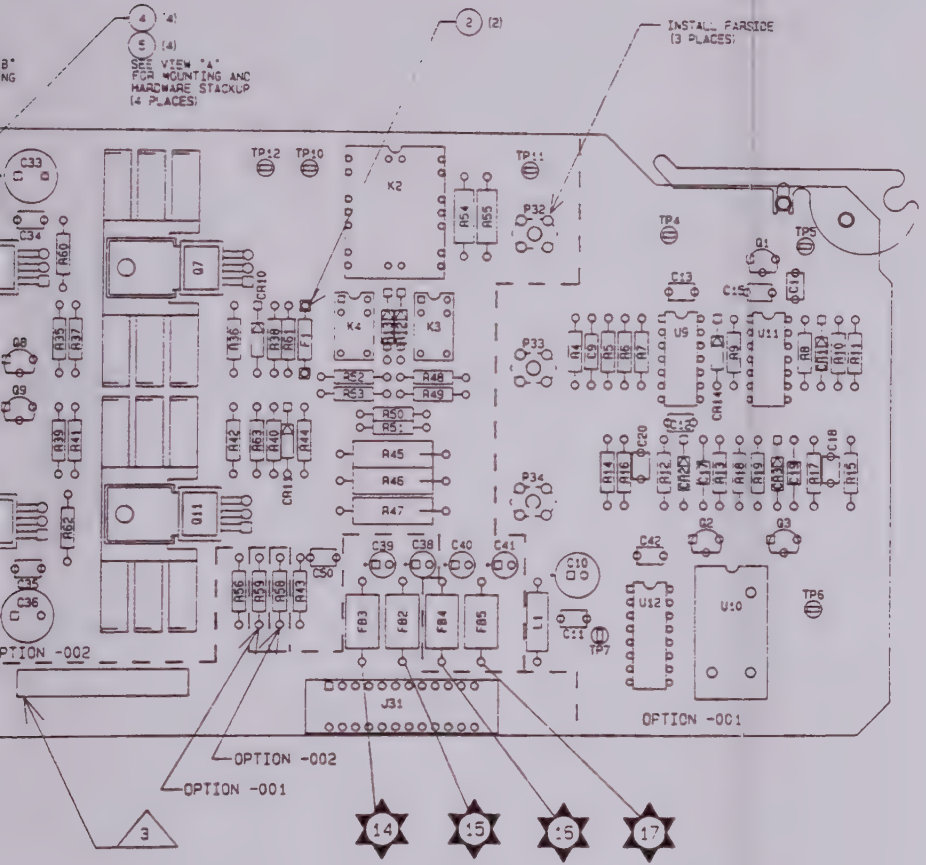



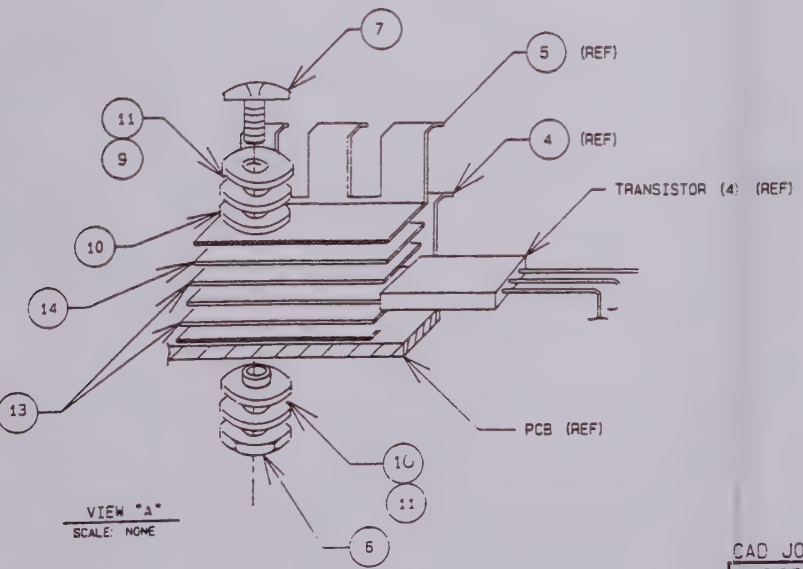

VIEW "B"
SCALE: NONE

4. TEST POINTS SHOWN AS (XX) ARE NOTATIONS FOR FAULT ISOLOATION PROCEDURES IN THE UNIT MAINTENANCE MANUAL.
5. ASSEMBLE PER WAVETEK WORKMANSHIP STANDARDS.
4. REFERENCE DESIGNATIONS DO NOT APPEAR ON PARTS.
3. MARK ASSEMBLY REVISION LETTER IN AREA SHOWN.
2. FOR ASSEMBLY INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 1004-00-0596.
1. SEE 1104-00-3386 FOR SCHEMATIC.

NOTE UNLESS OTHERWISE SPECIFIED

| REV | ECO | BY | DATE | APP |
|---|---|---|---|---|
| D | [illegible] | [illegible] | [illegible] | [illegible] |




VIEW "A"
SCALE: NONE

CAD JOB #: B0598

| | | |
|---|---|---|
| REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN Ro Fisher | DATE 6/27/90 |
| MATERIAL | CHECKED L Ash | 7/24/90 |
| FINISH WAVETEK PROCESS | PROJ ENGR [illegible] | 7/24/90 |
| DO NOT SCALE DRAWING | RELEASE APPROV [illegible] | 7/24/90 |

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE
FRACTIONS DECIMALS ANGLES
.XX ± .02 ±1°
.XXX ± .010

WAVETEK SAN DIEGO, CALIFORNIA

TITLE
PCA, AUXILIARY BOARD

| SIZE | FSCM NO | DWG NO | REV |
|---|---|---|---|
| D | 23338 | 1101-00-3386 | B |

SCALE 1.5 : 1 | MODEL 90/95 | SHEET 1 OF 1

1101-00-3386 B

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| REFERENCE DESIGNATORS | PART DESCRIPTION | ORIG-MFGR-PART-NO | MFGR | WAVETEK NO | QTY/PT |
|---|---|---|---|---|---|
| NONE | A/D AUX BD HIGH VOLT/IN-OUT REFERENCE | 1101-00-3386 | WVTK | 1101-00-3386 | 1 |
| NONE | SCHEMATIC, AUX BD 90/95 | 1104-00-3386 | WVTK | 1104-00-3386 | 1 |
| NONE | ASY ASSY, COAX J32 | 1200-00-3381 | WVTK | 1200-00-3381 | 1 |
| NONE | ASSY, COAX J33 | 1200-00-3382 | WVTK | 1200-00-3382 | 1 |
| NONE | COAX ASSY, J34 | 1200-00-3383 | WVTK | 1200-00-3383 | 1 |
| 14 | THERMAL SPREADER | 1400-02-3095 | WVTK | 1400-02-3095 | 4 |
| C27 | CAP CER 10PF 200V 5% AXIAL | CAC02C0G100J100A(OBS) | CORNG | 1500-01-0006 | 1 |
| C1 C11 C12 C13 C14 C15 C18 C2 C20 C22 C23 C24 C25 C26 C29 C3 C31 C34 C35 C4 C42 C5 C50 C6 C7 C8 | CAP CER MON .1MF 50V Z5U +80/-20% RAD LD SP .2 SP .2 | SR215E104ZAA | AVX | 1500-01-0420 | 26 |
| C21 | CAP CER 33PF 200V 5% AXIAL | CAC02C0G330J100A(OBS) | CORNG | 1500-03-3006 | 1 |
| C17 C19 | CAP CER 47PF 200V 5% AXIAL | CAC02C0G470J100A(OBS) | CORNG | 1500-04-7006 | 2 |
| C9 | CAP, CER, 470PF, 100V, 5% , AXIAL | CAC03C0G471J100A | CORNG | 1500-04-7100 | 1 |
| C38 C39 C40 C41 | CAP, ELECT, 10MF/25V RADIAL LEAD, SP .10 | NRE 10/63 | NIC | 1500-31-0002 | 4 |

| WAVETEK PARTS LIST | TITLE | ASSEMBLY NO. | REV |
|---|---|---|---|
| | PCA, AUX BD, OPT 001&002 | 1100-00-3389 | K |



| REFERENCE DESIGNATORS | PART DESCRIPTION |
|---|---|
| P32 P33 P34 P36 | CONN, SUB MIN |
| U10 | OSCILLATOR, TEMP COMPENSATED 10MHZ XTAL, 14 PIN DIP, 0.030 LEADS |
| F1 | FUSE, 1/4, 125V (PC) |
| 3 | PC BD EJECTOR |
| 4 | HEATSINK, TO-202, HORIZONTAL MOUNT |
| NONE | HEATSINK, TO-202 |
| 6 | NUT, HEX, 2-56, Z |
| 7 | SCREW, 2-56X1/2, PHP, Z |
| 5 | WASHER, FLT #6, .187 OD, .141 ID, .047THK, NYLON |
| 9 | WASHER, FLAT, CAD I, #2 |
| 10 | WASHER, SHOULDER, #2 SCREW |
| NONE | WASHER, LOCK, SPLIT S/S #2 |

WAVETEK PARTS LIST | TITLE PCA, AUX BD, OPT 001&002

| REFERENCE DESIGNATORS | PART DESCRIPTION | ORIG-MFGR-PART-NO | MFGR | WAVETEK NO. | QTY/PT |
|---|---|---|---|---|---|
| C33 C36 | CAP, ELECT, 100MF, 35V RADIAL LEAD, SP .20 | NRE101M35V10X12.5(OBS) | NIC | 1500-31-0102 | 2 |
| C37 | CAP, ELEC, 100 MF, 16V, RAD, .1 LS | NRE101M16V6.3X11 | NIC | 1500-31-0111 | 1 |
| C30 C32 | CAP, MET POLY, .1MF, 50V | 104MSS0AJK | IC | 1500-41-0413 | 2 |
| C28 | CAP, VARI, 7-35 pF, 160V. | 3004488603(OBS) | STNER | 1500-53-5010 | 1 |
| C10 | CAP, TANT, 22MF, 15V | 196D226X9015KA1(OBS) | SPRAG | 1500-72-2601 | 1 |
| 1 | PCB, AUX BD REF: SPEC 0008-00-0455 REV E | 1700-00-3386 | WVTK | 1700-00-3386 | 1 |
| L1 | INDUCTOR, 390MH | 2300-08 | DELVN | 1800-00-0023 | 1 |
| J31 | CONN, HEADER, 24 PIN, RECPT, 2X12, .1 CTR, PCMT | 0-0102384-7(REF ONLY) | AMP | 2100-02-0255 | 1 |
| J30 | CONN, HEADER, 40 PIN, RECPT, 2X20, .1 CTR PCMT | 1-0102385-2(REF ONLY) | AMP | 2100-02-0256 | 1 |
| 2 | SOCKET, MINISERT | 75060-013 | BERG | 2100-03-0076 | 2 |
| TP12 TP3 TP6 | TEST POINT, BLK, PC | TP-104-01-00 | COMPO | 2100-04-0054 | 3 |
| TP1 TP10 TP11 TP2 TP4 TP5 TP7 TP8 TP9 | TEST POINT, RED, PC | TP-104-01-02 | COMPO | 2100-04-0055 | 9 |

WAVETEK PARTS LIST | TITLE PCA, AUX BD, OPT 001&002 | ASSEMBLY NO. 1100-00-3389 | REV K



| REFERENCE DESIGNATORS | PART DESCRIPTION |
|---|---|
| 6 | RIVET PLASTIC |
| FB1 FB2 FB3 FB4 FB5 | BALUN CORE, FERRITE, 680 OHMS |
| 13 | INSULATOR, THERMAL W/CONDTVE ADHSIV COAT, FOR TO-202 PKG |
| K1 K3 K4 | RELAY, 1 FORMC, 3V, .312W, .295W |
| K2 | RELAY, SWITCH HIGH FREQ., 50ohm, 3V |
| R32 R33 | POT, SIDE TRIM, 20T, 100 |
| R22 | RES, MF, 1/8W, 1%, 1K |
| R43 R44 | RES, MF, 1/8W, 1%, 10K |
| R30 | RES, MF, 1/8W, 1% T2 4.99K |
| R21 | RES, MF, 1/8W, 1%, 9K |
| R4 R6 | RES, MF, 1/8W, 1%, 100 |
| R10 R5 R8 R9 | RES, MF, 1/8W, 1%, 1K |
| R35 R36 R41 R42 | RES, MF, 1/8W, 1%, 10 |

WAVETEK PARTS LIST | TITLE PCA, AUX BD, OPT 001&002

NOTE UNLESS OTHERWISE SPECIFIED

| REV | ECO | BY | DATE | APP |
|---|---|---|---|---|

| RIG-MFGR-PART-NO | MFGR | WAVETEK NO | QTY/PT |
|---|---|---|---|
| 7-948 | AMPH | 2100-07-0011 | 4 |
| 40082A1 | MONIT | 2300-99-0026 | 1 |
| 53.230 | LITFU | 2400-05-0042 | 1 |
| 7-2-C | BRIT | 2800-07-0032 | 2 |
| 30AB | EG&G | 2900-11-0037 | 4 |
| 71AB | EG&G | 2800-11-0038 | 4 |
| -56 HEX NUT | CMRCL | 2800-14-2100 | 4 |
| -56X1/2 PH | CMRCL | 2800-18-2108 | 4 |
| 515 | SMITH | 2800-26-0002 | 2 |
| AE-2 | CMRCL | 2800-26-2000 | 4 |
| 2SWS0202 | MICRO | 2800-27-0010 | 8 |
| 535338-134 | MS | 2800-45-2000 | 8 |

| ASSEMBLY NO. | 1100-00-3389 | REV K |
|---|---|---|
| PAGE 3 | | |

| REFERENCE DESIGNATORS | PART DESCRIPTION | ORIG-MFGR-PART-NO | MFGR | WAVETEK NO. | QTY/PT |
|---|---|---|---|---|---|
| R15 | RES. MF, 1/8W, 1%, 1.21K | RN55D-1211F | TRW | 4701-03-1211 | 1 |
| R24 | RES. MF, 1/8W, 1%, 1.5K | RN55D-1501F | TRW | 4701-03-1501 | 1 |
| R25 | RES. MF 1/8W, 1%, 1.96K | RN55D-1961F | TRW | 4701-03-1961 | 1 |
| R29 R30 R37 R38 R39 R40 | RES. MF, 1/8W, 1%, 21.5 | RN55D-21R5F | TRW | 4701-03-2159 | 6 |
| R39 | RES. MF, 1/8W, 1%, 2.21K | RN55D-2211F | TRW | 4701-03-2211 | 1 |
| R18 | RES. MF, 1/8W, 1%, 249 | RN55D-2490F | TRW | 4701-03-2490 | 1 |
| R27 | RES. MF, 1/8W, 1%, 2.74K | RN55D-2741F | TRW | 4701-03-2741 | 1 |
| R28 | RES. MF RN55D 365 OHM 1% | 5043ED365R0F | MEPCO | 4701-03-3650 | 1 |
| R14 R16 | RES. MF, 1.8W, 1%, 46.4 | RN55D-46R4F | TRW | 4701-03-4649 | 2 |
| R12 R19 | RES. MF, 1/8, 1%, 499 | RN55D-4990F | TRW | 4701-03-4990 | 2 |
| R36 R7 | RES. MF, 1/8W, 1%, 4.99K | RN55D-4991F | TRW | 4701-03-4991 | 2 |
| R60 R61 R62 R63 | RES. MF, 1/8W, 1%, 49.9 | RN55D-49R9F | CORNG | 4701-03-4999 | 4 |
| R26 | RES. MF, 1/8W, 1%, 6.04K | RN55D-6041F | MEPCO | 4701-03-6041 | 1 |
| R31 R34 | RES. MF, 1/8W, 1%, 68.1 | RN55D-68R1F | TRW | 4701-03-6819 | 2 |
| R11 R20 R23 R58 | RES. MF, 1/8W, 1%, 750 | RN55D-7500F | TRW | 4701-03-7500 | 4 |
| R13 R17 | RES. MF, 1/8W, 1%, 825 | RN55D-8250F | TRW | 4701-03-8250 | 2 |

| WAVETEK PARTS LIST | TITLE PCA, AUX BD, OPT 001&002 | ASSEMBLY NO. 1100-00-3389 | REV K |
|---|---|---|---|
| | | PAGE 5 | |

| RIG-MFGR-PART-NO | MFGR | WAVETEK NO. | QTY/PT |
|---|---|---|---|
| 31-080551-05-0101 | FASTX | 2800-60-0008 | 2 |
| 743666671 | FARIT | 3100-00-0017 | 5 |
| 403-09AC-55 | BERGQ | 3100-00-0021 | 8 |
| 01E-M-DC9V | AROMT | 4300-00-0034 | 3 |
| 02ET-9V | AROMT | 4300-00-0037 | 1 |
| 3XR100 | BECK | 4609-90-0017 | 2 |
| N55E-10018 | MEPCO | 4701-02-1001 | 1 |
| N55E-10028 | MEPCO | 4701-02-1002 | 2 |
| N55E49918 | DALE | 4701-02-4991 | 1 |
| 023IE9K008 | MEPCO | 4701-02-9001 | 1 |
| N55D-1000F | TRW | 4701-03-1000 | 2 |
| N55D-1001F | TRW | 4701-03-1001 | 4 |
| 043ED10R100F | MEPCO | 4701-03-1009 | 4 |

| ASSEMBLY NO. | 1100-00-3389 | REV K |
|---|---|---|
| PAGE 4 | | |

| REFERENCE DESIGNATORS | PART DESCRIPTION | ORIG-MFGR-PART-NO | MFGR | WAVETEK NO. | QTY/PT |
|---|---|---|---|---|---|
| R3 | RES. MF, 1/8W, 1%, 90.9 | RN55D-90R9F | TRW | 4701-03-9099 | 1 |
| R48 R49 R52 R53 | RES. MFLM, 1/8W, 0.1%, 10 ohm | RN55E-10098 | MECEN | 4701-12-0100 | 4 |
| R54 R55 | RES. MF, 1/4W, 1%, 10 | RN60D-10R0F | TRW | 4701-13-1009 | 2 |
| R51 | RES. MFLM, 1/8W, 1%, 349K | CCF5534936F | DALE | 4701-13-3491 | 1 |
| R45 R46 R47 | RES. MFLM, 1/2W, 0.1%, 1.47K | CMF-601471BT9 | DALE | 4701-32-1471 | 3 |
| CR14 | DIODE, ZENER, 6.8V | 1N754A | MOT | 4801-01-0754 | 1 |
| CR5 CR6 | DIODE, ZENER 9.1V, GLASS SILICON, 500MW | 1N5239 | TEL | 4801-01-5239 | 2 |
| CR1 CR4 CR7 CR8 CR9 | DIODE, HIGH CONDUCTANCE, ULTRA FAST | 1N5282 | FAIR | 4801-01-5282 | 5 |
| CR10 CR11 CR12 CR13 | DIODE, SWITCHING, GP, 100V, 200MA | 1N4148 | NSC | 4807-02-6666 | 4 |
| CR2 CR3 | DIODE 5082-2811 SCHOTTKY, 15V, 20MA | 5082-2811 | HP | 4809-02-2811 | 2 |
| Q1 Q3 Q8 | TRANS 2N3904 NPN GENERAL PURPOSE TO-92 | 2N3904 | FAIR | 4901-03-9040 | 3 |
| Q2 Q9 | TRANS 2N3906 PNP GENERAL PURPOSE TO-92 | 2N3906(DBS) | FAIR | 4901-03-9060 | 2 |

| WAVETEK PARTS LIST | TITLE PCA, AUX BD, OPT 001&002 | ASSEMBLY NO 1100-00-3389 | REV K |
|---|---|---|---|
| | | PAGE 6 | |

| REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN | DATE | WAVETEK San Diego, California |
|---|---|---|---|
| MATERIAL | CHECKED | | TITLE |
| | PROJ ENGR | | PARTS LIST AUXILIARY BOARD |
| FINISH WAVETER PROCESS | RELEASE APPROV | | |
| DO NOT SCALE DRAWING | UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES .XX ± .XXX ± | | SIZE D / FSCM NO 23338 / DWG NO 1100-00-3389 / REV K / SCALE / MODEL 90 / SHEET 1 OF 2 |

4 3 2 1

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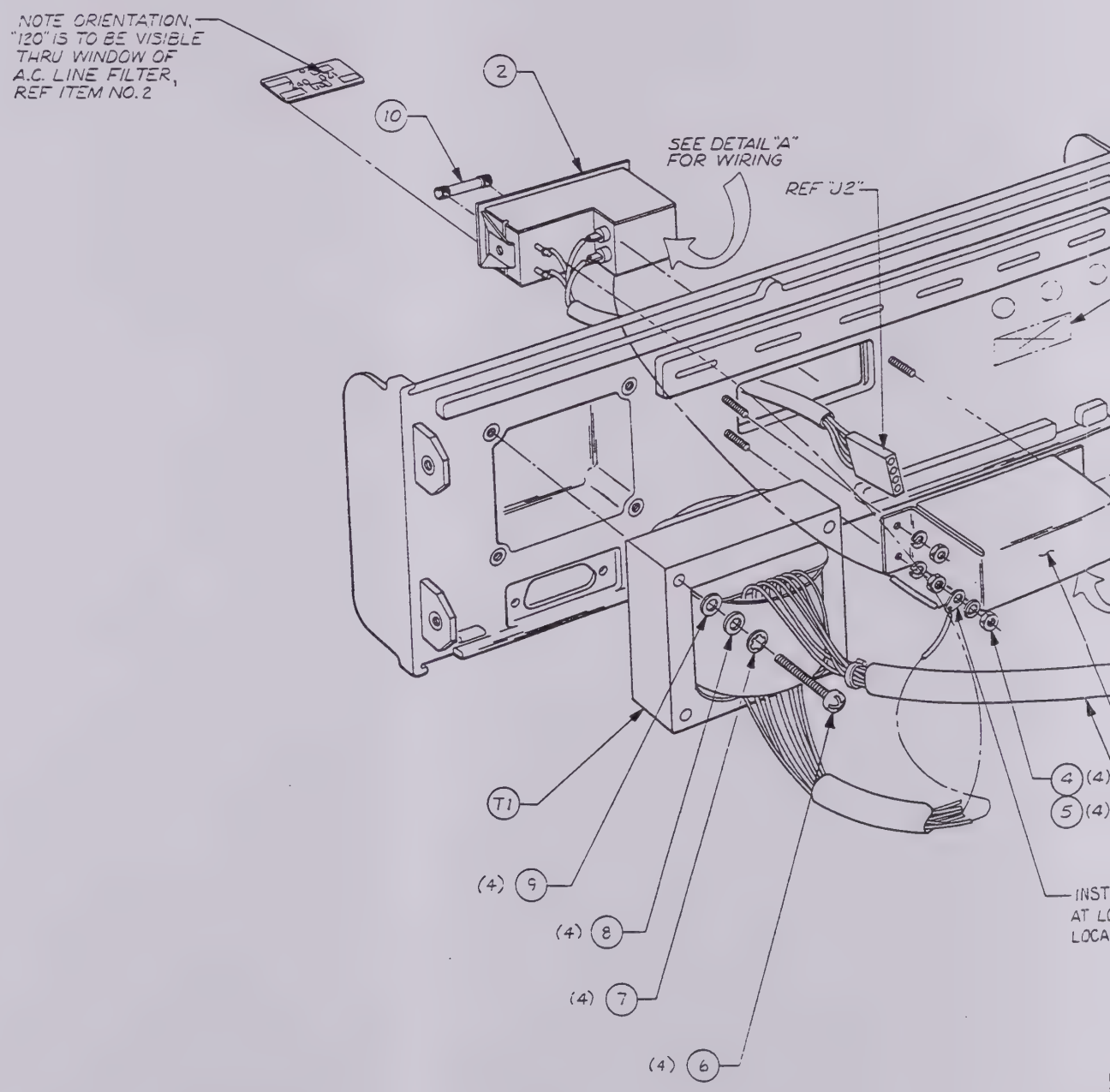
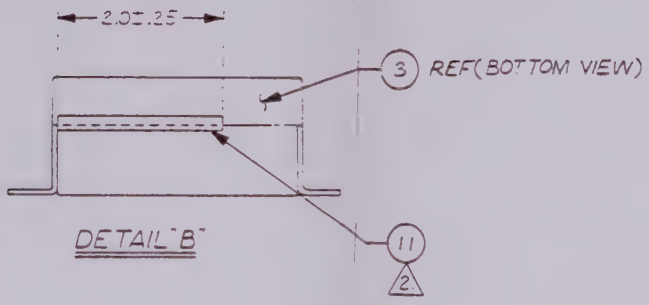



2. INSTALL GROMMET 3200-06-0079 (LESIG PART 924) OR 3200-06-0053 (MINOR RUBBER PART NO. ZX-4064) OR EQUIV. TO SHIELD (ITEM 3) WITH ADHESIVE 1600-03-0013 (LOCTITE PART NO. 414) OR EQUIV.

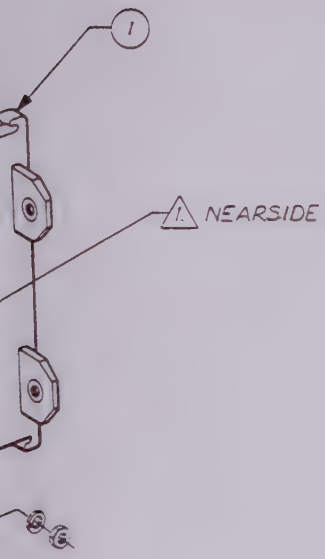
1. MARK ASSEMBLY NO. "1101-00-3325 " LATEST REV, FSCM 23338, PER MIL-STD-130, APPROX WHERE SHOWN.

NOTE UNLESS OTHERWISE SPECIFIED

| REV | ECO | BY | DATE | APP |
|---|---|---|---|---|
| A | ERC NO [illegible] | AP | | |
| B | ECO-[illegible] | | | |

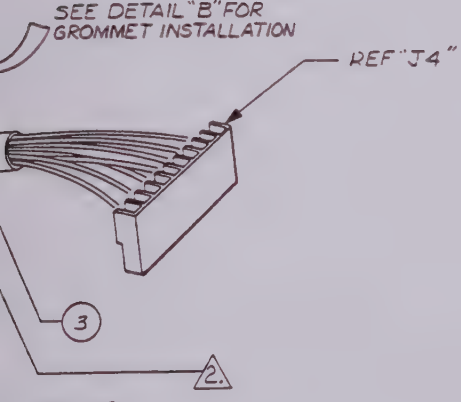



DETAIL "B"

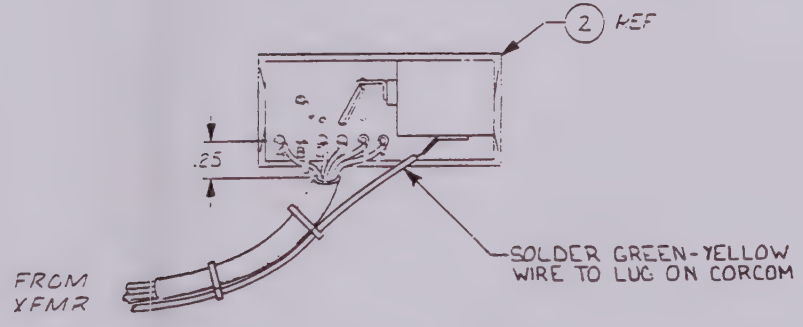



WIRE LIST

| XFMR WIRE COLOR | LINE FILTER TERM MARKING |
|---|---|
| VIOLET | A |
| BLUE | C |
| GRAY | D |
| WHT/BLK | E |
| WHT/GRAY | F |




LL GND LUG
VER MOUNTING
ON.




DETAIL A
XFMR WIRE HOOKUP

SEE SEPARATE PARTS LIST

| | | | |
|---|---|---|---|
| REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN SCIAP | DATE 3/7/90 | WAVETEK |
| MATERIAL | CHECKED D. Gutell | 4/5/90 | TITLE ASSEMBLY. REAR PANEL |
| FINISH WAVETEK PROCESS | PROJ ENGR | 4/5/90 | |
| DO NOT SCALE DRAWING | RELEASE APPROV. | | SIZE D · FSCM NO 23338 · DWG NO 1101-00-3325 · REV B |
| | UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES .XX ± .XXX ± | | SCALE: NONE · MODEL 90/95 · SHEET 1 OF |

1101-00-3325 B

4 3 2 1

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D

C

B

A

NOTE UNLESS OTHERWISE SPECIFIED

8 7 6 5

| REV | ECO | BY | DATE | APP |
|---|---|---|---|---|

| REFERENCE DESIGNATORS | PART DESCRIPTION | ORIG-MFGR-PART-NO | MFGR | WAVETEK NO. | QTY/PT |
|---|---|---|---|---|---|
| NONE | A/D. REAR PANEL ASSY. MODEL 90 | 1101-00-3325 | WVTK | 1101-00-3325 | 1 |
| 2 | CABLE ASSY. LINE FILTER | 1207-00-3011 | WVTK | 1207-00-3011 | 1 |
| 3 | SHIELD. AC CONN | 1400-02-3463 | WVTK | 1400-02-3463 | 1 |
| NONE | REAR PANEL. MODEL 90 | 1400-02-3035 | WVTK | 1400-02-3035 | 1 |
| NONE | FUSE. 1A. 250V. S-B | MDL 1 | BUSS | 2400-05-0029 | 1 |
| 4 | NUT. HEX. 4-40 | MS35649-244 | COML | 2800-14-4100 | 4 |
| 9 | WASHER. #8 FIBER DIN 470 | #8 FIBER WASHER | CMRCL | 2800-28-8000 | 4 |
| NONE | SCREW. PAN. CAD I. CROSS RECESS. 8-32 X 2 1/4 | 8-32 X 2 1/4 PAN | CMRCL | 2800-38-8136 | 4 |
| 5 | WASHER. LOCK REG. S/S #4 | MS 35338-135 | CMRCL | 2800-43-4000 | 4 |
| 8 | WASHER. #8. FLT. SS. THK .030. ID .174. OD .375 | 2800-46-8000 | CMRCL | 2800-46-8000 | 4 |
| 7 | WASHER. #8. INT TOOTH. LOCK. SS | 2800-56-0002 | CMRCL | 2800-56-0002 | 4 |
| 11 | EXTRU. RUBBER. U CHNL. 1/16 INSIDE. 1/8 OUTSIDE | 924 | LESIG | 3200-06-0079 | 2 |

| WAVETEK PARTS LIST | TITLE REAR PANEL ASSY. MODEL 90 | ASSEMBLY NO. 1100-00-3325 | REV C |
|---|---|---|---|
| | | PAGE 1 | |

| REFERENCE DESIGNATORS | PART DESCRIPTION | ORIG-MFGR-PART-NO | MFGR | WAVETEK NO. | QTY/PT |
|---|---|---|---|---|---|
| T1 | TRANSFORMER. POWER. 90/95 | 5600-00-0030 | ENSIG | 5600-00-0030 | 1 |

| WAVETEK PARTS LIST | TITLE REAR PANEL ASSY. MODEL 90 | ASSEMBLY NO. 1100-00-3325 | REV C |
|---|---|---|---|
| | | PAGE 2 | |

| REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN | DATE |
|---|---|---|
| MATERIAL | CHECKED | |
| | PROJ ENGR | |
| | RELEASE APPROV | |
| FINISH WAVETEK PROCESS | UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES .XX ± .XXX ± | |
| DO NOT SCALE DRAWING | | |

WAVETEK SAN DIEGO, CALIFORNIA

TITLE
PARTS LIST
REAR PANEL

| SIZE | FSCM NO | DWG NO | REV |
|---|---|---|---|
| D | 23338 | 1100-00-3325 | C |
| SCALE | | MODEL 90 | SHEET 1 OF 1 |

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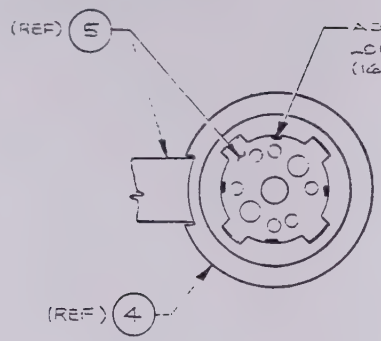
...RIGHTS BELONGING TO WAVETEK AND MAY NOT
...PRODUCED FOR ANY REASON EXCEPT CALIBRATION,
...RATION AND MAINTENANCE WITHOUT WRITTEN AU-
...ORIZATION

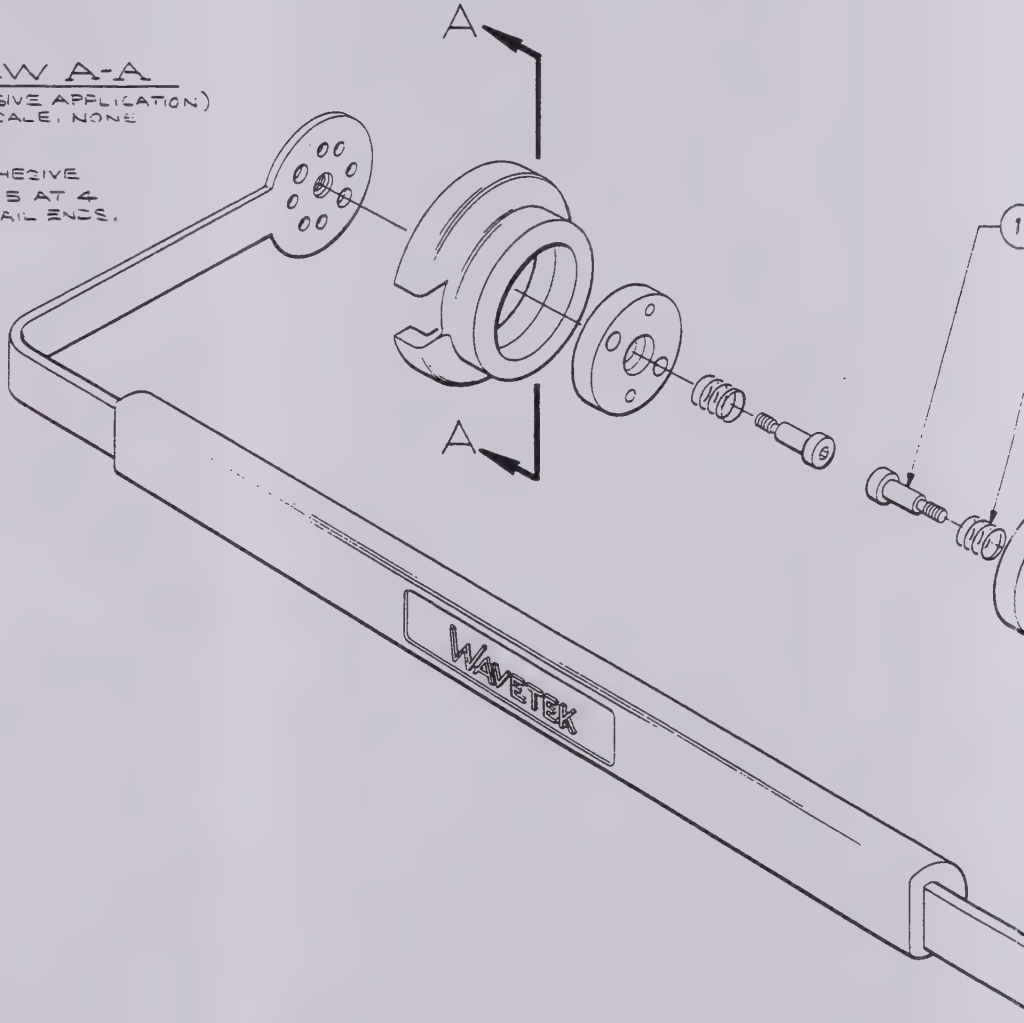



**ADHESIVE HANDLING PRECAUTIONS**

1. BONDS SKIN IN SECONDS. IN CASE OF BODY CONTACT, FLUSH WITH WATER. TO SEPARATE SKIN, SOAK IN HOT SOAPY WATER.
2. EYE IRRITANT. USE WITH ADEQUATE VENTILATION & USE EYE PROTECTION. IN CASE OF EYE CONTACT, BATHE THE EYE WITH LARGE QUANTITIES OF WATER (GET MEDICAL ATTENTION).

## VIEW A-A
(ADHESIVE APPLICATION)
SCALE: NONE

ADHESIVE APPLICATION:
USE MINIMUM AMOUNT OF ADHESIVE (1 DROP) BETWEEN ITEMS 4 & 5 AT 4 LOCATIONS SHOWN ON BOTH BAIL ENDS.



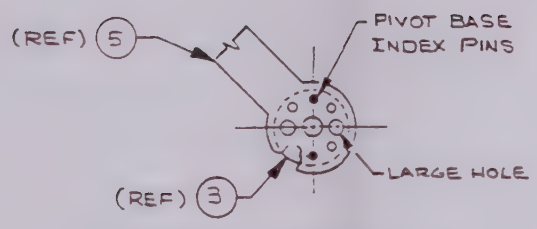

⚠1 MOUNTING SCREWS AND END CAPS ARE INSTALLED AT CHASSIS ASSEMBLY LEVEL. (EACH END)

NOTE UNLESS OTHERWISE SPECIFIED

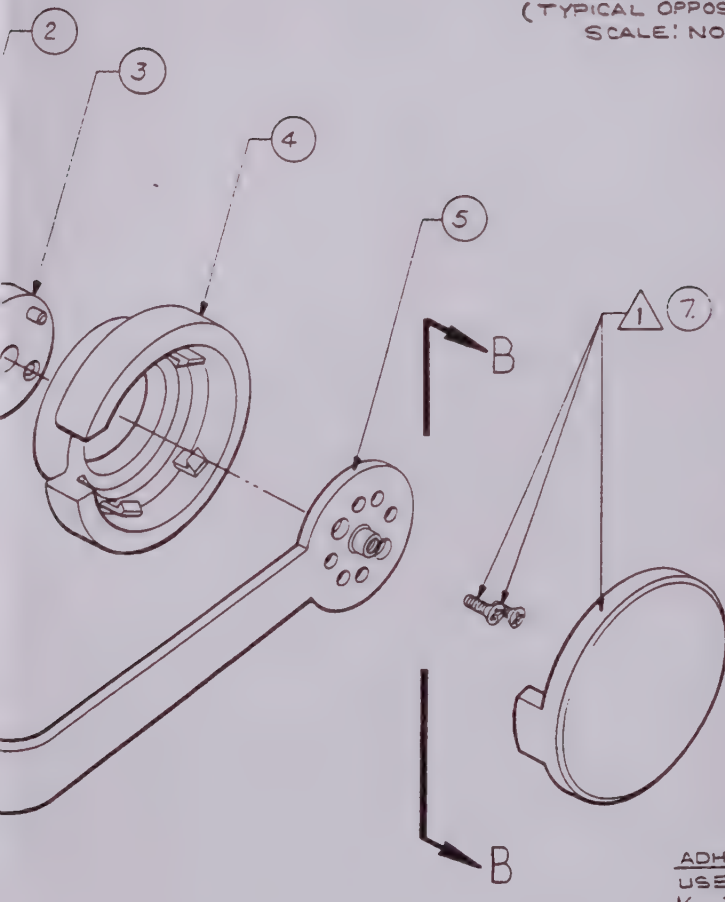
D C B A

8 7 6 5

| REV | ECO | BY | DATE | APV |
|---|---|---|---|---|
| A | ERO NO. 90-881 | AD | [illegible] | [illegible] |
| B | ECO # 90-[illegible] | MS | [illegible] | [illegible] |




ASSEMBLY ORIENTATION
(TYPICAL OPPOSITE SIDE)
SCALE: NONE




VIEW B-B
(ADHESIVE APPLICATION)
SCALE: NONE

ADHESIVE APPLICATION: (2 PLACES)
USE MINIMUM AMOUNT OF ADHESIVE APPROX 1/16 INCH DIA x 3/16 INCH LONG 2 PLACES AS SHOWN. ASSEMBLE PARTS WITHIN 5 MINUTES AFTER ADHESIVE APPLICATION.

| | | | |
|---|---|---|---|
| REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN D. COOPER | DATE 5-11-90 | WAVETEK SAN DIEGO, CALIFORNIA |
| MATERIAL | CHECKED | | TITLE: ASSEMBLY TILT BAIL |
| FINISH WAVETEK PROCESS | ENGR APPROV | | SIZE D · FSCM NO 23338 · DWG NO 1201-00-3392 · REV B |
| DO NOT SCALE DRAWING | RELEASE APPROV | | SCALE NONE · MODEL 90/95 · SHEET 1 OF 1 |

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES .XX .XXX

1201-00-3392 B

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C

B

A

NOTE UNLESS OTHERWISE SPECIFIED

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| REV | ECO | BY | DATE | APD |
|---|---|---|---|---|

| REFERENCE DESIGNATORS | PART DESCRIPTION | ORIG-MFGR-PART-NO | MFGR | WAVETEK NO. | QTY/PT |
|---|---|---|---|---|---|
| NONE | A/D TILT BAIL | 1201-00-3392 | WVTK | 1201-00-3392 | 1 |
| 3 | PIVOT BASE | 1400-02-3057 | WVTK | 1400-02-3057 | 2 |
| 4 | PULL COVER, BASE | 1400-02-3060 | WVTK | 1400-02-3060 | 2 |
| 5 | TILT BAIL GRIP | 1400-02-3061 | WVTK | 1400-02-3061 | 1 |
| 6 | PULL COVER CAP | 1400-02-3063 | WVTK | 1400-02-3063 | 2 |
| 7 | SCREW, 4-40*3/8, FHP, 82 DEG, Z, SELF-LOCKING | P32AS440R10Z | NYLOK | 2800-19-4108 | 2 |
| 1 | SHOULDER SCREW, HEX, 10-32 THREAD 3/8" DIA 10-32 SHOULDER SCREW | PZ-22-3 | BERG | 2800-23-0036 | 2 |
| 2 | SPRING, OD 360 L= 5 | LC-026E-1 | LEE | 2800-31-0004 | 2 |

| WAVETEK PARTS LIST | TITLE: TILT BAIL ASSY | ASSEMBLY NO. 1200-00-3392 | REV C |
|---|---|---|---|
| | | PAGE 1 | |

| | | | |
|---|---|---|---|
| REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN / DATE | WAVETEK San Diego, California | |
| MATERIAL | CHECKED | TITLE: PARTS LIST TILT BAIL | |
| | PROJ ENGR | | |
| FINISH: WAVETEK PROCESS | RELEASE APPROV | | |
| DO NOT SCALE DRAWING | UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ±1/32 DECIMALS .XX ±.02 .XXX ±.010 ANGLES ±1° | SIZE D / FSCM NO 23338 / DWG NO 1200-00-3392 / REV C | |
| | | SCALE / MODEL 90 / SHEET 1 OF 1 | |

D C B A

4 3 2 1

## A.1 Model 90

The Model 90 is a rugged 1mHz to 20 MHz programmable, synthesized Function Generator. The function generator produces predefined sine, triangle, and square waveforms. Waveforms can be continuous, triggered, gated, burst, AM (amplitude modulation), SCM (suppressed carrier modulation), FM (frequency modulation) or sweep modes. Balanced or unbalanced output are programmable from 1mV to 30 Vpp with selectable output impedances. An optional high voltage output supplies outputs of up to 40 Vpp.

At frequencies above 20 Hz (all functions – Continuous, AM, and SCM modes) the Model 90 phase locks its function generator to its internal frequency synthesizer (internal phase lock) which improves the frequency accuracy to ±(10 ppm + 1.5 ppm/°C); also see Option 001. Also the Model 90 can phase lock to an external source (same conditions as internal phase lock). When locked to an external source, the phase of the Model 90 output can be varied ±180°. In addition, the internal frequency synthesizer acts as an accurate internal trigger source for the trigger, gate, or bust modes.

## A.2 Specifications

### A.2.1 Waveforms (Functions)

Programmable sine, triangle, and square; variable symmetry for pulse and ramp waveforms, and dc.

#### Sine Distortion

All outputs, Sine function:
<1% (-40 dB) THD 1mHz to 20 Hz;
<0.5% (-46 dB) THD 20 Hz to 100 kHz.

Unbalanced Output, 50Ω and 75Ω, no harmonics above:
-40 dBc, 100 kHz to 2MHz,
-30 dBc, 2MHz to 6MHz,
-25 dBc, 6MHz to 20 MHz.

#### Time Symmetry

When time symmetry is fixed at 50%, the accuracy is <±(0.2% + 5 ns). Time symmetry is variable from 5% to 95% in 1% steps to 2 MHz and the limits linearly decrease to a fixed 50% at 20 MHz. Accuracy is <±(1% + 5 ns).

#### Square Transition Time

The transition time (rise/fall) is <9 ns, 10% to 90%, unbalanced output into 50 Ω impedance.

#### Aberrations

Overshoot and ringing is <(5% + 20 mV) of the peak to peak amplitude.

#### Triangle Linearity

10% to 90% nonlinearity:
±1%, 2mHz to 100 kHz;
±2%, 100 kHz to 2MHz;
±10%, 2MHz to 5MHz.

### A.2.2 Operational Modes

#### Continuous

In this mode the Model 90 supplies a continuous waveform at the selected frequency. The unit automatically selects its internal synthesizer at frequencies above 20 Hz.

#### Triggered

In this mode the Model 90 remains quiescent at trigger baseline of selected function until a trigger event occurs (positive-going transition at the Trig/Freq In connector, Manual Trigger, GPIB trigger command, or internal trigger rate generator). This initiates a single waveform at the programmed frequency and, after completing the waveform, returns the generator to the quiescent baseline value ready for another triggering cycle. Internal or external phase lock is disabled in the triggered mode. The generator can also be triggered using the internal trigger synthesizer. Accuracy of triggered waveform period is <±3%.

#### Gated

In this mode the Model 90 functions the same as the Triggered mode, except the generator runs continuously

while the triggering signal is true. The generator starts and stops in the quiescent state, and the Model 90 always complete its last cycle. Internally generated gating cycles have an approximate 1:1 on/off cycle.

### Burst

In this mode, the Model 90 functions the same as the Triggered mode, except that the number of cycles generated, when triggered, is programmable from 1 to 1,000,000. The generator starts and stops in the quiescent state.

### Amplitude Modulation (AM)

In this mode, the Model 90 functions the same as the continuous mode except an external signal modulates the instantaneous amplitude of the selected carrier from 0 to 100% AM. Average amplitude is as programmed except that maximum amplitude is limited to one-half its continuous value.

### Suppressed Carrier Modulation (SCM)

In this mode, the Model 90 functions the same as the AM mode, except the selected function (carrier) is suppressed to zero amplitude until an external signal is applied. Three scale factors (Vout/Vin) aid in determining the input to output signal level. SCM can only be selected when the Continuous signal level is <7.5 Vpp.

### Frequency Modulation (FM and VCG)

In the FM mode, an external signal controls the frequency of the generator. Connecting a dc level to the Mod In connector shifts the generator to a frequency based on the magnitude of the level. Connecting an AC signal to the Mod In deviates the frequency of the generator about its programmed frequency. The Model 90 only can be frequency modulated a maximum of three decades on a fixed range. Internal or external phase lock is not selectable in this mode.

### Sweep

In this mode, the Model 90 frequency, linearly or logarithmically, sweeps between programmable start and stop frequencies of up to three decades on a selected range. The Model 90 provides five sweep modes: sweep start, sweep stop, continuous sweep, triggered sweep, or manually sweep. Sweep time can be programmed from 100 ms to 3600s. Start/Stop frequency accuracies are <±3% within the top decade, and ±5% accurate on the lower two decades of the three decade sweep range. All 50% symmetrical waveforms can be swept.

## A.2.3 Frequency

### Range

1mHz to 20 MHz,
20 Hz to 20 MHz, synthesized,
1mHz to 1MHz, 600Ω (Balanced, Unbalanced, and High Voltage Outputs).

### Resolution

4 digits.

### Accuracy

±10 ppm (20 ±5°C) synthesized:
20 Hz to 20 MHz Continuous, AM, or SCM modes.

±3% of setting non-synthesized:
1 mHz to 20 Hz in Continuous, AM, or SCM mode;
1 mHz to 20 MHz, in Triggered, Gated, or Burst mode.
±3% of setting at 100:1 of range , linearly increasing to ±13% at 1000:1 of range in FM or Sweep mode.

### Stability

VS temperature:
±2 ppm/°C for synthesized (0°C to 50°C);
<100 ppm/°C for non-synthesized.

VS time:
±20 ppm/year for synthesized,
±0.5% for non-synthesized within 24 hours,
±0.1% for non-synthesized within 10 minutes.

### Internal Phase Lock

The Model 90 can be phase locked at frequencies >20 Hz (continuous, AM or SCM mode) to an internal crystal referenced frequency synthesizer which improves the generator's frequency accuracy and stability. A front panel annunciator (UNLOCK) indicates phase lock conditions.

### External Phase Lock

The Model 90 can be phase locked at frequencies >20 Hz (continuous, AM or SCM mode) to an external phase lock signal. Model 90 measures the external signal, sets the generator's frequency, and locks the generator to the source. When external phase locked, the external source controls the generator's frequency, stability and purity.

Also, external phase lock permits programing the phase angle relative to the positive-going zero crossing of the external sine wave. Phase angle may be set from ±180° (± π radians) with 1° resolution and, in the range of 50 Hz to 10 MHz, ±(4° + 20 ns) accuracy. If the external signal has dc offset, the Model 90 ignores the offset and phase lock referenced to the "0°" point on the external sine wave.

### A.2.4 Amplitude

#### Range

1mVpp to 15Vpp terminated into selected output impedance;

2mVpp to 30Vpp into an open circuit.

#### Resolution

4 Digits: 2mVpp to 20Vpp Open Circuit (1mV minimum),
1mVpp to 10 Vpp Terminated;

4 1/2: 20 Vpp to 30 Vpp Open Circuit,
10 Vpp to 15 Vpp Terminated.

Resolution may be reduced when the waveform is offset.

#### Accuracy

All functions at 1kHz, % of setting:
±(2% + 1mV), to 100 mVpp terminated;
±(2% + 2mV), to 1Vpp terminated;
±(2% + 10mV), to 15 Vpp terminated.

#### Flatness (50Ω or 75Ω)

Relative to 1kHz:
Unbalanced 50Ω
<2MHz
±0.3 dB, sine and square;
±0.5 dB, triangle.
2MHz to 20 MHz
±0.75 dB, sine and square;
±1.5 dB, triangle.
Balanced 135Ω
<100 kHz
±0.3 dB, sine.
100 kHz to 1MHz
±0.75 dB, sine.

### A.2.5 Offset

#### Range

±7.5 V terminated;
±15 V open circuit.

#### Resolution

4 digits; may be reduced if both offset and waveform amplitude are programmed.

#### Accuracy

±(2% + 1mV), to 9.99 mV terminated;
±(2% + 2mV), to 999 mV terminated;
±(2% + 10 mV), to 7.5V terminated.

### A.2.6 Outputs

#### Sync Output

Sync Out is a female BNC connector which supplies a TTL compatible pulse output at programmed frequency and symmetry in phase with the square function. Output level is >2Vpp to <0.4 Vpp into 50Ω termination. The 10% to 90% transition times are less than 13 ns.

#### Sweep Output

Sweep Out is a female BNC connector, which supplies a 0 to +5V ramp to indicate sweep position. Source impedance is 600Ω . Inactive when not in Sweep Mode.

#### Unbalanced Output

Unbalanced output is a female BNC connector which is the source of programmed waveform at selected frequency, amplitude, symmetry, and offset. Source impedance is 600Ω ± 1% to 1 MHz, 50Ω ± 1%, or 75Ω ± 1% to 20 MHz. Not available when the Balanced output is selected.

#### Balanced Output

Balanced outputs are dual "banana jack" connectors which provide differential outputs of the selected function at programmed frequency, amplitude and symmetry. A universal binding post is provided for signal common "center tap" connection. Source impedance is programmable as 135Ω ± 1% or 600Ω ± 1% to 1 MHz. Not available when the Unbalanced output is selected.

### A.2.7 Inputs

#### Trigger/Lock Input

Trig/Lock In is a female BNC connector which serves two functions. The source can be TTL (dc to 20 MHz)

or bipolar (0.6 Vpp to 30 Vpp, 20 Hz to 20 MHz (default)). Minimum pulse width is 50 ns. Trigger source is hardware selectable; refer to paragraph 2.4.6

In phase lock, Trig/Lock In accepts the signal that phase locks the Model 90 to the external source. The Model 90 measures the frequency, sets the unit to match the source frequency, and phase locks the generator to the source. Model 90 phase locks range is 20 Hz to 20 MHz in the Continuous, AM or SCM modes. The input signal must be a sine wave or bipolar signal (600 mVpp to 30 Vpp).

Input impedance is 10 kΩ ± 2%.

### Modulation In

Mod In, a female BNC connector, serves as the modulation input for FM (VCG), AM, and SCM. Input impedance is 10 kΩ ±2%. Bandwidth is dc to 1MHz. Maximum input level is ±20 Vpp (into 10 kΩ).

FM Mode: In FM an external signal provides linear control of waveform frequency around the programmed frequency. A ±10V input signal causes a 1000:1 frequency change (selected frequency range is the top decade in a possible three decade frequency span). An AC signal varies the frequency around the programmed frequency. A dc level sets the generator to a single frequency. VCG bandwidth is dc to 100 kHz limited by 0.06 V/µs maximum slew rate. FM bandwidth is dc to 100 kHz deviation rate; with maximum envelope distortion of 1.78% (-35 dB) taken with 10 MHz carrier frequency, 1kHz modulation frequency and 1MHz (10%) depth (sine wave modulation).

AM Mode: In the AM mode an external signal provides linear control of waveform amplitude around the programmed amplitude value. Displayed amplitude dependent scale factor specifies approximate Vpp (into 10 kΩ) required for 100% modulation. AM bandwidth is dc to 1MHz; with a maximum envelope distortion of 2% taken with 1MHz carrier frequency, 1 kHz modulation frequency and 70% AM (sine wave modulation).

SCM (Suppressed Carrier Modulation): In the SCM mode, an external signal linearly controls the waveform's amplitude about the zero carrier level. The Model 90 displays a scale factor (2V/V, 0.2V/V, or 0.02V/V) which defines the amount of Mod In signal level to produce a SCM output level. SCM bandwidth is dc to 1MHz. Maximum envelope distortion is 2% (1MHz carrier and 1kHz modulation).

## A.2.8 Display

The Model 90 contains a 16 digit, Vacuum Florescent Display (VFD) with 14 segment, alphanumeric characters and 11 mm character height. All selectable parameters display the parameter name, the numeric value and the unit. In addition, the display shows GPIB messages, various utilities, maintenance and diagnostic information.

## A.2.9 GPIB Programming

### Address

Valid GPIB addresses for the Model 90 are 0-30 (default address is 9), front panel selectable and battery backed-up.

### Subsets

SH1, AH1, SR1, RL1, PP0, DC1, DT0, C0, T6, L4, TE0, LE0 and E1.

## A.3 Options

**001: Frequency Reference** — This option improves the reference frequency from an adjustable crystal to an adjustable TCXO with a ±1 ppm performance over the operating temperature range. A rear panel REF IN connector accepts TTL or Bipolar sine wave (>500 mVpp at 10 MHz) reference input. The REF OUT connector provides TTL compatible 10 MHz pulses capable of driving a 50Ω termination.

**002: High Voltage Output** – This option provides a rear panel connector which supplies all functions at programmable amplitude levels from 1mVpp to 40 Vpp with a maximum output frequency of 1MHz. Source impedance is less than 5Ω, and the receiving device must have an input impedance of greater than 500Ω.

Amplitude Accuracy
- ±3% + 1mV to 400 mVpp
- ±3% + 2mV to 4Vpp
- ±3% + 10 mVpp to 40 Vpp

Flatness: ±1dB.

Square Wave Rise/Fall :<160 ns at full output.

Sine Harmonics: -30 dB to 1MHz.

**003: Handles and Rack Adapter** — This option consists of a pair of handles and rack adapters that attach to the left and right sides of the Model 90. The rack adapters allow the instrument to be mounted in a standard 19 inch rack. Also included are a pair of handles which may be installed in place of the existing front panel corner pieces.

**004: Extended Cards** – This option supplies a set of extender cards which provide access to the daughter boards during maintenance.

Recommended Spare Parts - A recommended spare parts package for the Model 90 can be obtained from Wavetek by ordering Wavetek part number 1200-00-3462.

## A.4 General

### A.4.1 Physical Specifications

#### Dimensions

35.6 cm (14.in.) wide, 13.3 cm (5.219 in.) high and 43.2 cm (17 in.) deep.

#### Weight

Approximately 7.7 kg (17 lb.) net; 11.8 kg (26 lb.) shipping.

#### Power

90 to 108, 108 to 126, 198 to 231, or 216 to 252 Vrms; 48 to 440 Hz; 1 phase; <110 VA.

### A.4.2 Environmental Specifications

The Model 90 conforms to MIL-T-28800C, class 5.

**Temperature Range**
0°C to +50°C for operation;
–40°C to +70°C for storage.

**Warm Up Time**

Allow 20 minutes for specified operation at ambient temperature of last Autocal ±10°C. Autocal should be performed when the ambient temperature has changed.

**Operational Humidity**
11°C to 30°C at 95% relative humidity;
31°C to 40°C at 75% relative humidity;
41°C to 50°C at 45% relative humidity.

**Altitude**
To 10,000 ft. (3050m.) for operation;
To 15,000 ft. (4570m.) for non-operating.

**Vibration (Operating)**
Vibration level of 0.013 in. from 5 to 55 Hz (2g acceleration at 55 Hz.).

**Shock (Non-operating)**

40g, 9ms half-sine wave.

**Bench Handling (Operating)**

4 in. or point of balance drop, any face, solid wooden surface.

#### Electromagnetic Compatibility

The Model 90 has been tested to MIL-STD-461A Notice 4 (EL) and meets the emission and susceptibility requirements of CE02, CE04, CS02, CS06, RE02, RE02.1, and RS03.

### Phase Calibration Using an Oscilloscope

This procedure provides an alternate method of Model 90 phase calibration. Simply use the following steps in place of Steps 16, 17, 18, and 19 of the calibration procedure (section 4).

### Step 16 Adjust Phase 0°

1. The Model 90 displays PHASE 0 XXXXX where XXXXX represents a calibration value. Connect the test equipment as shown in figure B-1.
2. Set the signal source controls as follows:
   Set Function to Sine.
   Frequency to 2.01 kHz.
   Output Level to 5Vpp.
3. Set the scope controls as follows: Trigger to channel 1.
   Adjust Channel 1 and 2 gain and offset controls so identical superimposed waveforms are displayed.
   Select channel 2 Invert.
   Select 1 and 2 Add.
4. On the Model 90,
   Adjust the Knob to null the waveform on the scope.
   Press the ⟹CURSOR key. Verify that the display flashes CALIBRATING for then displays PHASE +180 XXXXX. Pressing ⟹CURSOR key stores the calibration value in internal memory.

### Step 17 Adjust Phase +180°

1. The Model 90 displays PHASE +180 XXXXX where XXXXX represents a calibration value. Leave the test equipment connected as shown in figure B-1. Do not change the signal source.
2. Set the scope controls as follows:
   If necessary, adjust Channel 1 and 2 gain and offset controls so identical superimposed waveforms are displayed.
3. On the Model 90,
   Adjust the Knob to null (minimum displayed signal) the added waveform on the scope display.
   Press the ⟹CURSOR key advance to the next step. Verify the display flashes CALIBRATING and then displays PHASE –180 Y XXXXX. Pressing ⟹CURSOR key stores the calibration value in internal memory.

### Step 18 Adjust Phase -180°

1. The Model 90 displays PHASE -180 XXXXX where XXXXX represents a calibration value. Leave the test equipment connected as shown in figure B-1. Do not change the signal source. The scope should not need adjustment.
2. On the Model 90,
   Adjust the Knob to null (minimum displayed signal) the waveform on the scope display.

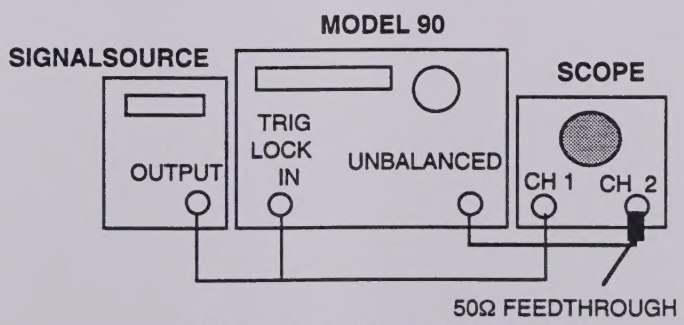


**Figure B-1. Phase Setup**

Press ⟹CURSOR key to advance to the next step. Verify that the display flashes CALIBRATING and then displays SQ PHASE 0 XXXXX. Pressing ⟹CURSOR key stores the calibration value in internal memory.

### Step 19 Adjust Square Phase 0°

1. The Model 90 displays SQ PHASE 0 XXXXX where XXXXX represents a calibration value. Leave the test equipment connected as shown in figure B-1. Do not change the signal source.

2. Set the scope controls as follows:
   Turn off Add.
   Observe the sine wave reference on channel 1.
   Trigger on channel 1.
   Observe the square wave on channel 2.
   Superimpose the sine over the square wave.
   Increase the gain of channel 1 (sine) by 10.
   Using the scope controls, adjust channel 1 for 0Vdc offset.
   Using the scope horizontal time and trigger slope, set the negative-going zero crossing of the sine wave and square wave to occur at the center of the graticule. Magnify the center of the display by X10.

3. On the Model 90,
   Adjust the Knob to null so the squares transition passes through the sine's zero crossing point.

4. Set the scope as follows:
   Change the trigger slope to display the positive-going transition. If an error exists, split the difference between the two slopes using the knob.

5. On the Model 90,
   Press the ⟹CURSOR key to advance to the next step. Verify the display flashes CALIBRATING and then displays CONFIDENCE. Pressing ⟹CURSOR key stores the calibration value in internal memory.

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